ELECTROPLATED MULTI-PATH COMPLIANT COPPER INTERCONNECTS FOR FLIP-CHIP PACKAGES

A Dissertation
Presented to
The Academic Faculty

by

Raphael Ifeanyi Okereke

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
George W. Woodruff School of Mechanical Engineering

Georgia Institute of Technology
May 2014

Copyright © 2014 by Raphael Ifeanyi Okereke

ELECTROPLATED MULTI-PATH COMPLIANT COPPER INTERCONNECTS FOR FLIP-CHIP PACKAGES

Approved by:

Dr. Suresh K. Sitaraman, Advisor
School of Mechanical Engineering
Georgia Institute of Technology

Dr. I. Charles Ume
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Todd Sulchek
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Madhavan Swaminathan
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Muhannad S. Bakir
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: December 09, 2013

In memory of my Dad

ACKNOWLEDGEMENTS

I would like to first express my deepest gratitude to my parents, Ambrose Ikechukwu Okereke and Happiness Chima Okereke for their guidance and love through the years leading up to this and for their encouragement through this journey.

I would also like to thank my advisor, Dr. Suresh Sitaraman for giving me an opportunity to work with him and learn from him. His advice and support both on and off the job have been truly invaluable. I feel fortunate for having Dr. Sitaraman as my mentor and guide over the years at Georgia Tech, and it has been a wonderful experience. I would like to thank my thesis committee, Dr. Ume, Dr Swaminathan, Dr. Sulchek and Dr. Bakir for being a part of my thesis committee, for their insightful comments in steering the direction of my thesis and for the time taken reviewing my write-up.

I wish to thank my labmates in the Computer Aided Simulation of Packaging Reliability (CASPaR) Lab, particularly, Justin Chow, Nicholas Ginga, Xi Liu, Greg Ostrowicki, Sathyanarayanan Raghavan, and Christine Taylor. Their friendship and support over the years have been invaluable in the completion of this work. I would like to thank the members of the Packaging Research Center (PRC) for their support through the Next-Generation-Substrate fabrication cleanroom and test equipment for the characterization of my test structures. I would also like to acknowledge the members of the Mixed Signal Design group under Dr. Swaminathan for their assistance in designing test features for the electrical characterization of my devices. I would like to acknowledge the members of the Institute for Electronics and Nanotechnology for their support through the Marcus and Pettit nanotechnology cleanrooms.

I would like to acknowledge the National Science Foundation (Grant No. ECCS-0901679) as well as Qualcomm Inc. for supporting this work.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS IV

LIST OF TABLES VIII

LIST OF FIGURES IX

SUMMARY XV

CHAPTER 1: INTRODUCTION 1

CHAPTER 2: REVIEW OF COMPLIANT INTERCONNECTS 9

2.1. Introduction 9

2.2. Scope 9

2.3. First level interconnections 9

2.4. Compliant Interconnections 16

CHAPTER 3: OBJECTIVES AND APPROACH 31

3.1. Gaps with Existing Suite of Compliant Interconnect 31

3.2. Objectives 36

3.3. Approach 37

3.4. Scope of Research 38

CHAPTER 4: DESIGN SELECTION 39

4.1. Introduction 39

4.2. Design Approach 41

4.3. Multi-path Compliant Interconnects 42

CHAPTER 5: MECHANICAL AND ELECTRICAL MODELING METHODOLOGY 49

5.1. Introduction 49

5.2. Material Modeling 49

5.3. Mechanical Compliance Simulation 53

5.4. Thermo-Mechanical Stress/Strain Modeling 54
5.5. Electrical Simulations 60
CHAPTER 6: DESIGN OF THREE-PATH DELTA INTERCONNECT 63
6.1. Introduction 63
6.2. Delta interconnects 63
6.3. Parametric Analysis 64
6.4. Characteristics of Selected Design 82
CHAPTER 7: FABRICATION OF COMPLIANT INTERCONNECTS 90
7.1. Micro-fabrication Overview 91
7.2. Photoresist Selection 92
7.3. Multi-path Interconnect Fabrication 94
CHAPTER 8: REFLOW OF ASSEMBLY DEVELOPMENT OF DELTA INTERCONNECTS ON ORGANIC SUBSTRATE 115
8.1. Introduction 115
8.2. Significance 115
8.3. Test Vehicle Design 116
8.4. Thermo-mechanical reliability assessment 117
8.5. Substrate Fabrication 119
8.6. Assembly Process Development 120
8.7. Assembly Yield Challenges and Process Enhancement 127
8.8. Assembled Interconnects 134
CHAPTER 9: EXPERIMENTAL CHARACTERIZATION AND RELIABILITY ASSESSMENT 136
9.1. Introduction 136
9.2. Electrical tests 136
9.3. Mechanical tests 144

9.4. Reliability Assessment 156

9.5. Failure Analysis 163

CHAPTER 10: HETEROGENEITY AND SCALABILITY OF DELTA INTERCONNECTS 165

10.1. Heterogeneity 165

10.2. Scalability of Delta Interconnects 175

10.3. Conclusion 179

CHAPTER 11: SUMMARY AND CONTRIBUTIONS 180

11.1. Summary 180

11.2. Findings and Contributions 181

11.3. Future Work 182

REFERENCES 183

LIST OF TABLES

Table 2-1: Copper pillars 17

Table 2-2: Polymer-Metal Hybrid Interconnects 19

Table 2-3: Nano-pillar interconnects 20

Table 2-4: Stress-released interconnects 23

Table 2-5: Leads on Compliant Supports 25

Table 2-6: Serially Fabricated Interconnects 27

Table 2-7: 3D compliant structures 29

Table 4-1: Simulation parameters of 2, 3 and 4 path interconnects 45

Table 4-2: Mechanical and Electrical performance of 2, 3 and 4 path interconnects 46

Table 5-1: Highlights of JEDEC JESD-A104D type J [63] 57

Table 6-1: Aspect ratio (AR) risk matrix based on photolithography 67

Table 6-2: Thermal cycling vs Thermal shock of Delta interconnects 77

Table 6-3: DC response of interconnects for resistance and inductance 87

Table 6-4: AC response of interconnects @ 1 GHz for resistance and inductance 87

Table 6-5: Properties of Delta Interconnects 89

Table 7-1: Constituents of copper sulfate plating bath per liter 103

Table 7-2: SRP220 reflow study 104

Table 7-3: Constituents of tin-silver plating bath per liter 110

Table 10-1: Heterogeneous interconnects: high, intermediate and low compliance Delta interconnect variants 166

Table 10-2: Measurement interconnect resistances by type 173

LIST OF FIGURES

Figure 1-1: RC delay as a function of gate length for Al/ SiO_2 vs Cu/Low-κ [2] 3

Figure 2-1: Wire-bonds between Die and Package [18] 10

Figure 2-2: Tape Automated Bonding [19] 12

Figure 2-3: Xerox flip-chip technology for high-density packaging [24] 16

Figure 4-1: Flex Connect 42

Figure 4-2: Evolution of the multi-path interconnects from G-Helix 42

Figure 4-3: Base design of the 2, 3 and 4 path interconnects 43

Figure 4-4: Description of interconnect's features 45

Figure 4-5: 2, 3 and 4 Path Interconnect's compliance response to variable orientation in-plane loading 47

Figure 5-1: Stress-strain response of modeled copper behavior at 2 different temperatures 50

Figure 5-2: Simplification of board composition/properties 52

Figure 5-3: Finite element setups for (a) out-of-plane compliance (b) in-plane compliance 53

Figure 5-4: In-plane compliance simulation setup 54

Figure 5-5: Left image is a picture of the full assembly. Right image is a cut-out strip (highlighted in white in left image) representing the portion of the assembly modeled for thermo-mechanical reliability assessment. 55

Figure 5-6: Generalized plane displacement model of a strip from the Interposer assembly. Interposer is hidden in right image to reveal interconnects 56

Figure 5-7: Hysteresis loop for ductile material 58

Figure 5-8: Temperature cycle profile used in thermo-mechanical simulations 59

Figure 5-9: ANSYS resistance measurement setup 61

Figure 5-10: Representation of resistor network for analytical calculation 62

Figure 6-1: Geometric details of Delta Interconnects 64

Figure 6-2: Delta interconnects in-plane compliance as a function of its cross-section... 68
Figure 6-3: Out of Plane Compliances... 70
Figure 6-4: Interconnects resistances for various beam cross-sections ... 70
Figure 6-5: FastHenry models for inductance simulations ... 71
Figure 6-6: Inductive response of interconnects for various beam cross-sections ... 72
Figure 6-7: Two observed interconnect failure locations based on finite element predictions... 73
Figure 6-8: Interconnect fatigue life based on highest strained element location ... 74
Figure 6-9: Interconnect fatigue life based on a common failure location ... 75
Figure 6-10: Solder fatigue life based on highest strained element location... 76
Figure 6-11: Plastic strain in solder bump comparison between a rapidly cooled assembly and a slowly cooled one... 77
Figure 6-12: Compliance vs Fatigue life as a function of beam width for various beam thicknesses ... 79
Figure 6-13: Fatigue life as a function of Compliance for explored geometries of Delta Interconnects... 79
Figure 6-14: Fatigue life of interconnect as a function of orientation ... 81
Figure 6-15: Default orientation of Interconnect for orientation dependent fatigue life study... 82
Figure 6-16: Full RL response of Interconnect up 20 GHz ... 83
Figure 6-17: Interconnect resistance for: No failures, 1 path failure and failure of 2 paths ... 84
Figure 6-18: Ansoft Q3D model for RLC characterization of the interconnects ... 86
Figure 6-19: First principal stress (MPa) in die at room temperature... 88
Figure 6-20: Die curvature at room temperature ... 88
Figure 7-1: SPR220-7 film thickness vs Spin speed curves for a 4" wafer... 93
Figure 7-2: Absorbance curves of exposed (lower curve) and unexposed SPR220 [70] . 94

Figure 7-3: Die layout 94
Figure 7-4: Interconnect mask width design increased to 6.6 μm to compensate for etch loss during release step 95
Figure 7-5: Fabrication of domed interconnects 96
Figure 7-6: Pro-Engineer®5.0 3D rendering of Interconnect 97
Figure 7-7: Fully released domed interconnect sample 98
Figure 7-8: Image of developed photoresist showing pad openings 100
Figure 7-9: Copper plating bath setup 101
Figure 7-10: Optical image of plated daisy chain 103
Figure 7-11: Profile of dome with an inverted peak 105
Figure 7-12: Interconnect delamination as a result of poor adhesion to copper pad 106
Figure 7-13: Polymer domes on daisy chains (metallized for SEM) 106
Figure 7-14: Cross-section of domes showing relative profile heights 107
Figure 7-15: Ruptured dome as a result of excess pressures built-up beneath metal dome caps due to large thermal excursion of sample 108
Figure 7-16: Interconnects with extended center pads to avoid wetting of interconnects during solder reflow or during assembly to bumped substrates 110
Figure 7-17: Interconnects with copper columns and plated solder 111
Figure 7-18: Images of released interconnect samples 113
Figure 7-19: Pre-reflowed and reflow solder bumps on compliant interconnects 113
Figure 8-1: Highlight of features embedded in test vehicle design 117
Figure 8-2: Test vehicle layout highlighting probing locations 119
Figure 8-3: Finetech flip-chip bonder 121
Figure 8-4: Placed die prior to assembly reflow 121
Figure 8-5: Reflow temperature profile used for assembly 124
Figure 8-6: Warpage comparison at solder reflow temperature between a balanced (left) and imbalanced copper substrates 125

Figure 8-7: Sheared off interconnects after assembly reflow cool down as a result of poor adhesion 128
Figure 8-8: Grossly overplated solder creating non-uniformity in overall interconnect heights 129
Figure 8-9: Edge of die showing no wetting of the substrate pads as a result of non-contact between interconnects and substrate pads 129
Figure 8-10: Image of damaged interconnects caused handling errors a) SEM pre-assembly micrograph b) X-ray inspected sample post assembly 130
Figure 8-11: Failure resulting from interconnect to substrate pad misalignment 131
Figure 8-12: Non-parallel vacuum chucks can lead to uneven pressure distribution on assembly 132
Figure 8-13: Post assembly observation of inclined die relative to substrate 132
Figure 8-14: Comparison of a) reflowed solder in an assembly to b) a failed reflow also in an assembly 133
Figure 8-15: Assembled interconnect 135
Figure 9-1: Four point measurement setup using probe station 137
Figure 9-2: CAD illustration of inbuilt four wire measurement structures in test vehicle 139
Figure 9-3: Electrical test structures for measuring the scattering parameters of the interconnects 140
Figure 9-4: Plots comparing simulated response against measured insertion loss (S21) 142
Figure 9-5: CAD model representing assembled fabricated structures characterized for electrical performance (the die is hidden in this view) 143
Figure 9-6: Interconnect pair with adjust properties to simulate response of interconnects alone 143
Figure 9-7: Simulated interconnect response based on full scale model material adjusted model 144

Figure 9-8: Out-of-plane compliance setup used in both physical tests and simulations 145
Figure 9-9: Load-displacement curve for high compliance interconnect 146
Figure 9-10: In-plane compliance setups used for a) simulations and b) physical tests. 146
Figure 9-11: Macro-samples created to enable the measurement of in-plane compliance 147
Figure 9-12: Macro-sample setup for compliance testing 148
Figure 9-13: Load versus displacement response of macro-samples............................ 149
Figure 9-14: Compliance results of macro-samples as a function of load orientation ... 150
Figure 9-15: Structural integrity tests checking adhesion of fabricated interconnects to the annular copper pads and to silicon 151
Figure 9-16: Measured assembled die curvature at room temperature compared with simulation.. 152
Figure 9-17: Plated test coupons @) 20 µm thick coupons on photoresist release layer b) 100 µm thick coupons on 500 nm thick titanium release layer 154
Figure 9-18: Comparison of thermal treatments on material response of test coupon ... 155
Figure 9-19: Thermal load profile used in thermal cycling of assembled samples 157
Figure 9-20: Test specimens within thermal cycle chamber 157
Figure 9-21: Status of daisy chains for monitored sample prior to thermal cycling....... 158
Figure 9-22: Resistance of corner interconnects over several thermal cycles 159
Figure 9-23: Failure distribution of interconnects 160
Figure 9-24: Thermal shock samples 161
Figure 9-25: Thermal shock fatigued samples... 162
Figure 9-26: X-ray inspection of failed interconnects 163
Figure 10-1: Topographical layout of heterogeneous implementation b) Mask design . 165
Figure 10-2: Strip model of heterogeneous interconnect layout (Die hidden) 167
Figure 10-3: First principal stress (MPa) in die at room temperature........................... 169
Figure 10-4: Out-of-plane die nodal displacement (mm) at room temperature. 169

Figure 10-5: Elemental accumulated total strain range for the third stabilized thermal cycle 170
Figure 10-6: Accumulated plastic strain range comparison between Delta interconnect variants 171
Figure 10-7: Interconnect layout on heterogeneous die 172
Figure 10-8: Load vs. displacement plot to determine out-of-plane compliance 174
Figure 10-9: Patterned photoresists over copper pads 175
Figure 10-10: Reflowed and metallized domes over copper pads 176
Figure 10-11: 100 µm fabrications showing three multi-path designs 176
Figure 10-12: Released 400 µm pitch fabrications without plated solder 178
Figure 10-13: Released interconnects with plated solder caps 178

SUMMARY

The international technology roadmap for semiconductors (ITRS) 2012 report foresees the use of porous dielectric materials with a low dielectric constant in conjunction with copper interconnects as a way to reduce the resistive-capacitive (RC) delay in microelectronic applications. However, the introduction of pores in the dielectric not only serves as stress raisers but also diminishes the structural strength of the material. The challenge therefore with the implementation of low-k dielectrics for high-performance flip-chip packages is to create a reliable die to organic substrate interconnect solution which induces low stresses on the die to prevent the cohesive cracking and the interfacial delamination of the dielectric material.

Potential interconnect solutions that meet this challenge are MEMS-like compliant freestanding micro-structures. These structures are designed to work as spring-like elements which allow the free lateral and out-of-plane motion between the silicon die and the organic substrate under assembly conditions as well as under thermal or power cycling. Thus, the focus of this research is to design, fabricate, and characterize electrically and mechanically an innovative compliant interconnect approach that addresses these challenges.

The proposed interconnect is scalable in dimensions and pitch, and consists multiple electrical paths which will provide redundancy against interconnect failure. The multi-path design employs parallel electrical paths which effectively split a larger cross-sectional area into several smaller areas making the overall design more compliant than otherwise. This research proposes wafer-level, high-yield, CMOS-compatible fabrication procedure using sequential photolithography and copper electroplating. The proposed interconnects are symmetric and are amenable to easy reflow assembly to substrates. The mechanical compliance of the fabricated structures is studied through nano-indentation, while the electrical characteristics are assessed through fabricated prototypes. The

thermo-mechanical reliability of compliant interconnects is also demonstrated. Lastly, the dimensional scalability of the interconnects is also demonstrated.

CHAPTER 1

INTRODUCTION

Electronic packaging or simply packaging has existed since the first passives were soldered to a board to make the first electronic devices such as radios. It refers to the connection of discrete electronic components to a system to facilitate communication among different components and thus to the entire system. Some of the functions of the electronic package are to provide electrical connectivity, structural protection and facilitate efficient thermal management. Furthermore, packaging also facilitates I/O redistribution from smaller pitch to larger pitch I/O interconnection thus accommodating different routing densities, as well as a mismatch in material properties. Over the years, electronic components have gradually been scaled down in size to improve performance and increase functionality. For example, in the 1990's electronic devices such as Walkmans, digital cameras, calculators and phones were all discrete devices. With today's refinements in technology, all of these functionalities have been integrated into a single device in a package that is a fraction of the size of the smallest of these earlier devices.

Miniaturization is therefore synonymous with today's microelectronics devices as a result of the benefits derived from smaller components. Such benefits include faster clock speeds, shorter signal transit times, [1] and lower power requirements per component, to mention a few. With respect to transistors, smaller transistors imply larger transistor densities and greatly increased switching speeds. This naturally leads to increased data throughputs requiring circuitry capable of handling such high bandwidths. To keep up with the data throughput, circuit designers have sought better conductors for use as electrical traces and materials with lower dielectric constants to improve the Resistive-Capacitive (RC) delay or time constant of signal transmission lines. This high

bandwidth demand motivated the transition from aluminum to copper-on-chip traces, as copper is 40% more conductive than aluminum.

An increase in conductivity alone is not enough to sustain the trends in chip performance. Figure 1 illustrates graphically the gain in performance by shifting from aluminum-based conductors with silicon dioxide dielectrics to copper conductors accompanied by low dielectric constant materials. The graph shows a marked improvement in delay for the newer copper/low-κ dielectric assembly over aluminum/ SiO_2, particularly at the finer node sets. Since RC delay is a product of electrical resistance and capacitance of the signal transmission lines, it became essential in the same wise to lower capacitance associated with these lines. The capacitance of a trace is dependent on the geometric details of the conductor, namely the surface area of the conductor, the dielectric constant of the insulator separating it from surrounding conductors and its proximity to neighboring conductors. The resistance of the trace, on the other hand, depends on the conductor material as well as its cross-sectional area. However at very high frequencies (in the gigahertz range), such as is common in high performance systems, the electrical resistance of the trace becomes increasingly dependent on the perimeter of the conductor as a result of skin effect. In this case, a conductor with a large perimeter will make for a lower resistance trace at high frequencies, but this also implies that it will have a large surface area, which can offset the gains in the reduction of resistance by increasing its capacitance. Taking into account also that the geometry and spacing of on-chip traces is decided by I/O density, there could be little wiggle room to alter the geometry of the traces in high-density circuitry. Basically, since the trace resistance and capacitance have an inverse dependence on the surface area of the conductor at high frequencies, it seemed necessary to look into the dielectric media as an avenue to lower on-chip interconnect delay.

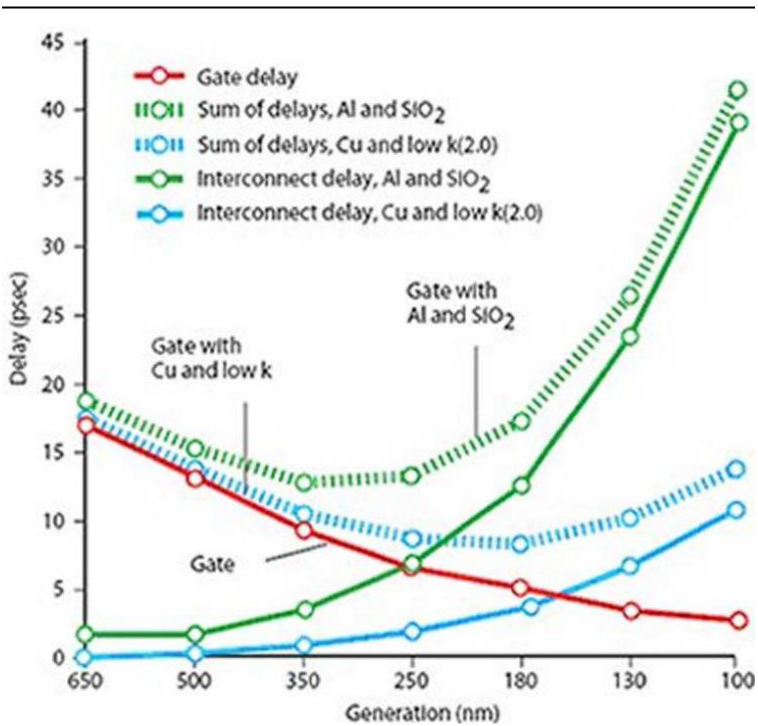


Figure 1-1: RC delay as a function of gate length for Al/ SiO_2 vs Cu/Low-κ [2]

Silicon dioxide (SiO_2) has been the dielectric of choice for earlier devices owing to its thermal stability, good mechanical strength, low coefficient of thermal expansion (CTE) and good adhesion strength. However, it has a dielectric constant of 3.9, therefore requiring materials with lower dielectric constant to address the RC delay. This led to the development of fluorosilicate glass (FSG) as a substitute with a relative dielectric constant of about 3.7 [3]. Further developments led briefly to the use of organic polymers, which were later abandoned due to their relative softness, high CTE and their propensity to delaminate [4].

Today, with technology nodes approaching the size of an atom, more aggressive reductions in the insulation's dielectric constants are needed. However, to reduce the dielectric constant to a minimum, dielectrics with values closer to those of free space which has a relative dielectric constant of 1 are needed. The International Technology Roadmap for Semiconductors (ITRS) 2012 report foresees porous dielectric materials as a solution to achieving materials with a dielectric constant of less than 2 [5]; however,

achieving this feat is not without challenges. At current levels, the introduction of porosity into a dielectric media to attain a dielectric constant of 2.4 or lower has been shown to exacerbate integration issues [6]. The introduction of nano-pores within the dielectric material not only lowers its mechanical strength but also acts as stress raisers within the material resulting in lower fracture strength.

In a traditional flip-chip package utilizing an organic substrate, the thermo-mechanical strains on solder interconnects as a result of the differential CTE between the silicon die and the organic substrate is counteracted with the application of an underfill. Underfills are typically composed of polymeric materials impregnated with inorganic fillers so as to match its CTE to that of the solder bumps. In so doing, the underfill acts as an extension of the solder bump, sharing the loads which would otherwise be solely borne by the solder, and in effect reducing damage to the solder bumps. However, this process tightly couples the die to the substrate inducing very high stresses within the die. These elevated stress levels are acceptable for packages utilizing SiO_2 as the dielectric media, but could be detrimental for packages employing low-κ materials as they could delaminate or crack due to their poor adhesion and low fracture strength [7].

As a direct consequence of the poor adhesion and low strength of low-κ materials, delamination and cracking of the back end of the line (BEOL) stack has become an increasingly prominent failure mode with traditional solder bump interconnects. Such “white bumps” occur during the reflow cool down of the assembly from the melt temperature of the solder to room temperature. During this cooldown, the CTE mismatch between the organic substrate and the die creates stresses in the die high enough to crack or delaminate the BEOL stack. In addition to the CTE mismatch and the temperature change during cooldown, the high stresses are induced due to the high stiffness of the solder bumps. The high stiffness of the solder bumps creates a mechanically tighter coupling of the die to the substrate.

To address these reliability issues, researchers have sought packaging solutions capable of lowering intrinsic stresses induced in the die/substrate assembly. With the realization that the introduction of underfilling in a flip-chip assembly is responsible for the high package stresses, a logical first step will be the elimination of the underfill or by substituting it with a compliant polymer. However, the removal of the underfilling renders the solder bumps vulnerable to premature fatigue failure as it no longer has the support of the underfill. Furthermore, the removal of the underfilling step does not address the white bump issue which occurs ever before the package is underfilled. Hence a compliant substitute for the otherwise rigid solder bumps is needed. This need led to the development of compliant interconnects as substitutes for solder bumps in packages requiring low stresses such as packages employing low-κ or ultra-low-κ dielectric layers. For the rest of this thesis, low-κ will be used to represent low-κ and ultra-low-κ materials.

Various compliant interconnect designs have been proposed such as G-Helix [8] [8], Elastec Bump [9], Stress-Engineered Interconnects [10], and Mechanically Flexible Interconnects [11] to list a few. With each design having its own strengths and weaknesses, it is difficult, if not impossible, to create an interconnect design that satisfies all expectations. It is foreseen that a logical path of approach to move this technology forward will be to create interconnect designs for specific applications. However, several issues remain to be addressed with this technology before it can be adopted into the mainstream as a potential solution into the low-κ fracture problem.

Truly compliant interconnects, in general, have higher electrical parasitics than solder bumps as a result of their comparatively longer and slender profiles. It is therefore natural to expect higher electrical parasitics for this technology. Any gains made in improving the compliance of the interconnect is usually offset by a degradation in its electrical parasitics and vice-versa. Fillion [12], Liao [13] and Kacker [14] proposed methods to address this issue. The first is the use of multipath structures in the place of single path conductors. This technique has been shown to be able to improve compliance

without degrading the electrical performance of the interconnect. The other method to address this bottleneck is to use designs of varying compliance where the interconnects at the center of the die have columnar structures with low compliance and low electrical parasitic, while the interconnects near the edge of the die have higher compliance and higher electrical parasitic. Such a heterogeneous architecture could potentially address both electrical and mechanical requirements [15]. Although such an architecture is helpful, it is still necessary to explore other design options for compliant interconnects such that their mechanical performance can be enhanced and possibly their electrical performance as well.

This work explores multipath interconnect designs that are not of pillar or column configuration such as those proposed by Liao [13] and Xu [16]. The methodology employed in the interconnect design starts with simulations using available material properties. Through a design of simulation type study, the critical parameters which include the interconnect's width and height were adjusted to come up with dimensions that meet thermo-mechanical reliability requirements. This work goes further to fabricate the interconnects, a critical step in its development. Through fabrication, the feasibility of the technology as a manufacturable interconnect solution is established which then provided opportunities to physically characterize the design.

While the original intent of the interconnect was as an off-chip interconnect, much effort has also been devoted into exploring its potentials as an interposer-to-board technology. Off-chip interconnects also known as level 1 interconnects are connections between the silicon die and interposer, while the interposer to board technology also known as a level 2 connection allows communication between interposer and board. Level 2 connections have typically employed ball grid arrays (BGA) comprised of solder balls as interconnects. However, with the pending shift from organic to silicon/glass interposer technology to accommodate ultra-fine pitch components at the first level, the

CTE mismatch originally encountered between a silicon die and an organic interposer is now moved to the interposer-board level.

In a system-on-package (SoP) type technology where die stacking is encouraged as a means of reducing die footprint, global trace lengths and hence signal transit times across dies, the aggregated stiffness of the combined die stack can make them extremely rigid and difficult to bend. For such an assembly, when stacked dies are mounted over an organic board, the non-compliance of the stack exacerbates the stresses borne by solder bumps, since the restricted warpage of the assembly provides no relief to the solder bumps in such a scenario. Since BGA packages are typically not underfilled, this can lead to premature fatigue of the solder balls at the second level.

Furthermore, for applications where the mounted devices are sensitive to vibration, i.e. such as in a MEMs type applications. The rigid interconnections provided by solder balls may transmit package vibrations to the sensitive sensory elements mounted over them. This can lead to noise coupling, distorting the acquired signal and hence impeding the sensory resolution of such a device. Lastly, depending on the size of die being assembled and the surface planarity of the organic board on which it is to reside, it is possible to eliminate the interposer level completely with compliant interconnects provided that the board design can handle the signal routing and I/O pitch.

In summary, numerous compliant interconnect solutions have been proposed by several researchers to address the low-κ reliability challenge introduced by using porous dielectrics. However, a solution truly capable of meeting the packaging requirement challenges associated with low-κ dies has not been achieved. Such a solution should be capable of sufficiently decoupling the organic board's thermally induced strains from those of the die without generating excessive reaction forces which can fracture the low-κ dielectric. The ideal solution will not only be capable of decoupling the die and substrate motions, but will also need to be reliable under static and cyclic loading. Most importantly, the interconnect should have good electrical properties such that it does not

become the bottleneck in high speed signaling circuits. The following section will outline some of the compliant interconnects that are being pursued at various academic and industrial institutions and the challenges associated with them.

CHAPTER 2

REVIEW OF COMPLIANT INTERCONNECTS

2.1. INTRODUCTION

The preceding chapter introduced the subject of electronic packaging and the motivation for an alternative type of interconnection for packages utilizing low-κ dielectric media as interlayer dielectric materials. However, to bring the current state-of-the-art into perspective, a history of existing technologies is reviewed, with a focus on the strengths and weaknesses of each design. This knowledge is insightful in the creation of a packaging solution capable of addressing contemporary and future challenges associated with the integration of ILDs.

2.2. SCOPE

This chapter explores the most prominent first level interconnects common in today's industry namely: wire-bonding, tape automated bonding and flip-chip bonding. These interconnect technologies have been around for a while now with each suited to a particular type of application. Their strengths and weaknesses are explored and the benefit of flip-chip packages including the compliant variants of this technology.

2.3. FIRST LEVEL INTERCONNECTIONS

2.3.1. Wire-bonding

Wire-bonding was invented in the 1950's by Bell labs [17] and has come a long way since its inception. It is the oldest form of off-chip interconnection in use today and is still the most popular (owing to a small extent industry's reluctance to deviate from a proven technology) but mostly because it can still meet the performance and connection requirements of today's devices. This technology utilizes fine wire to establish connections between the bond pads of a die to the package pads (Figure 2-1). To create these connections, a short length of the connecting wire is first reflowed into a sphere by

creating an arc across its tip. Then, using ultra-sonic energy, the ball is scrubbed against the die pad, which is traditionally coated with gold to form a gold-to-gold bond. The wire is then drawn out over to the package pad where a wedge bond is created completing the circuit, and its end clipped in preparation for the next connection. The described process is for a ball-to-wedge bonding traditionally used with gold wires and now copper wires.

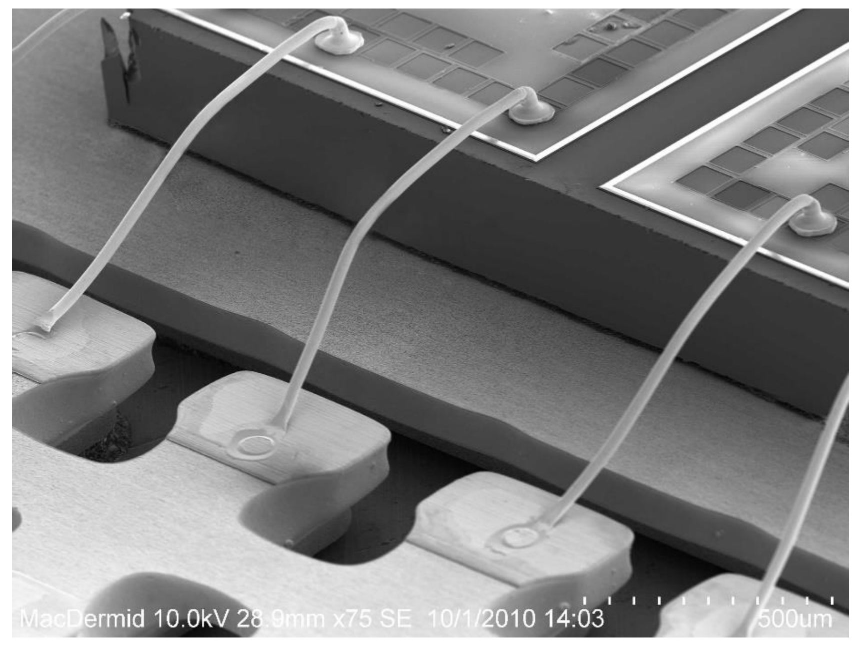


Figure 2-1: Wire-bonds between Die and Package [18]

Wire-bonding technologies have typically utilized gold-to-gold bonding for fine pitch requirements as gold was less prone to oxidation, easier to handle and allowed consistently good joints. Recently, motivated by the high cost of gold, a number of industries successfully transitioned from gold to copper wires, thereby reducing material costs by as much as 400 times at today's market rates. In addition to the lower cost, the selection of copper improves the conductivity of the wire by as much as 40%. This improvement in conductivity has extended the capability of wire-bonding into the high-performance application market.

Some key benefits of wire-bonding that has kept it as the preferred interconnection method include its versatility in being able to create connections between any die-to-package configuration. The relatively long length of the interconnecting wires

introduces compliance in the assembly, making these connections thermo-mechanically reliable.

While a good method of interconnection, wire-bonding has the following limitations keeping it from being a serious contender in the high performance market. It utilizes long leads to make connections across components. These long leads introduce large parasitics, which can degrade the quality of the signal. To accommodate the minimum pitch restriction required for wire-bonding, dies employing this technology are usually about a third larger than an equivalent flip-chip die [17]. This is due to the peripheral nature of wire-bond connections, as the bond pads need to fit along the edges of the die. The larger footprint requirement incidentally leads to increased cost as larger silicon dies are required, which can dramatically reduce the number of dies in a wafer batch. Furthermore, the sequential nature of wire-bonding makes it a slower option for assembly, and with industry's impending move to 450 mm wafers, wire-bonding may no longer be a contender for the lowest cost per connection.

2.3.2. Tape Automated Bonding

Tape automated bond (TAB) was introduced as a lower cost replacement of wire-bonding by providing a highly automated technique for packaging high I/O devices [17]. TAB utilized a flexible tape as substrate on which copper traces were patterned to match the die pads. Using adhesives or solder, the die is attached to the tape creating connectivity between the die pads and the copper leads on the tape.

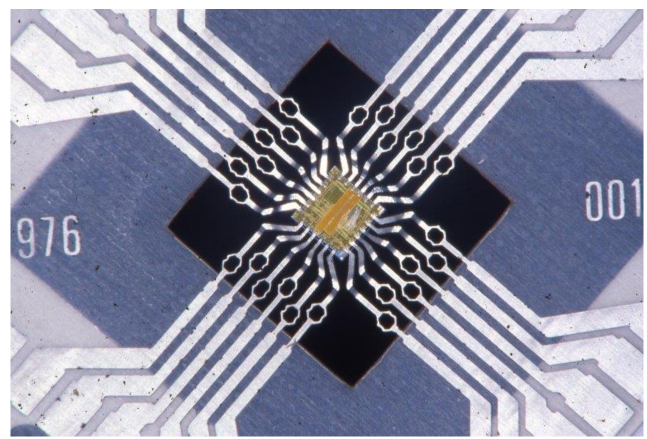


Figure 2-2: Tape Automated Bonding [19]

Some of the benefits derived from TAB include its ability to handle finer pitches than wire-bonding. A direct consequence of this is that TAB can handle higher I/O counts than wire-bonding. Most TAB layouts are peripheral in nature much like wire-bonding, however, configurations with an area-array layout can also be handled provided that the pitch is large enough to allow routing across the peripheral interconnects. Furthermore, as a result of its shorter leads, TAB assemblies tend to have superior electrical performance relative to wire-bonded assemblies and provide the added benefit of device burn-in prior to system integration.

A number of the drawbacks associated with this technology include the relative process inflexibility associated with the creation of the flex circuit. It introduces an added step in the assembly process which can be translated to cost. Package sizes tend to scale with the number of I/O's on the die in order to accommodate the outer lead pads [17]. Lastly, this technology provides no room to mount additional components such as passives on the tape or its backside.

2.3.3. Flip-Chip Technology

Flip-chip technology was developed in an attempt to create a cheaper, more reliable and a higher productive alternative to wire-bonding of the early era [17]. While developed originally for ceramic substrates by IBM Corp., the utility of this

interconnection technology has been greatly diversified. Flip-chip technology derives its name from its assembly process. The die to be assembled is flipped over a matching substrate such that its active side faces the substrate pads. The substrate or die pads usually include solder bumps which are reflowed to create an electro-mechanical connection between the die and the carrier (substrate).

With cost being a strong driver in the micro-electronics field, ceramic substrates were soon replaced with organic boards reinforced with fiber glass, such as FR4 boards. While these proved to be much cheaper, they created reliability issues in the assembly. The reliability failures were thermo-mechanically induced, and the source of the failures was the differing CTE between the organic boards and silicon. Organic substrates were originally designed to have their CTE matching those of the copper traces routed along their surface to prevent delamination. With a CTE of about 17 ppm/K, this created a large mismatch with the assembled die which has a CTE of about 3 ppm/K. In comparison with ceramic substrates with a CTE of about 6 ppm/K, the source of the thermo-mechanical reliability failures for solder bumps comes to light.

This led to the development of the underfill also by IBM to address the thermo-mechanical reliability challenges created in assemblies using organic substrates. To implement, underfill is dispensed at the interface between the die and the substrate to fill the gaps around the solder bumps. The underfill is then thermally cured. Functionally, the cured underfill acts as an extension of the solder bumps tightly coupling the die to the substrate. This in effect converts the die to substrate assembly separated by the solder bumps into a tri-layer material with the underfill and solder bumps acting as the third layer. The package now gains compliance through warpage of the assembly and the deformation load is distributed across these layers [20]. In effect, the thermally-induced deformation load that would otherwise have been borne solely by the solder bumps is now shared between the solder bumps and the underfill. This reduces the strains on the interconnects and thus prolongs the solder's fatigue life.

The use of underfill to create thermo-mechanically reliable packages has worked well since its introduction. Packages developed during the nascent stages of flip-chip packaging have typically used SiO_2 or Si_3N_4 as the dielectric of choice. SiO_2 is a thermally stable compound with excellent adhesion to silicon. The introduction of underfilling to such packages greatly increased the intrinsic stresses in the assembly, but these packages were able to handle these stresses because of the structural strength of the dielectric and its excellent adhesion. However, the need for faster interconnects that can handle the data throughput of modern electronic chips led to the development of low-κ materials which can reduce the capacitance of on-chip interconnects. Reducing the capacitance of the interconnects reduces signal propagation delays by lowering the time constant of the circuit.

As discussed in chapter 1, very few naturally occurring materials have dielectric constants of less than 3. Recent efforts to drive down the dielectric constants below 2.5 achieve this by incorporating voids within the dielectric media. There are two common methods currently employed in producing porous dielectrics. The first is a template approach and the second is a sol-gel process. In the template approach, the pores within the dielectric are created by co-depositing a sacrificial compound which is thermally decomposable with the dielectric media. After deposition, the sacrificial material is thermally decomposed to create pores within the dielectric. The sol-gel process uses hydrolysis and polycondensation of alkoxides to form porous low-κ films [21]. In either case, the dielectrics produced from both approaches have low cohesive strength and poor adhesion to the base substrate.

Therefore when underfilling is introduced to such packages the outcome could be catastrophic. Cracking of the low-κ dielectric and delamination are the two common failures that have been observed. In several instances, these mostly occur during the assembly reflow process. As the assembly cools from the reflow temperature down to

room temperature, the stresses in the connecting solder creates high enough stresses on the die to fracture or delaminate the low-κ dielectric [22, 23].

For this reason researchers and scientists alike have sought new off-chip interconnection methods to lower the magnitude of stresses induced on the die to prevent dielectric failure. Such a solution should avoid underfilling if possible, as underfilling is an additional process step, and it usually contributes to high thermo-mechanical stresses in the die. Also, underfilling makes the die non-reworkable. The solution for such an interconnect gave rise to compliant interconnect structures.

The earliest known compliant interconnect happened to be the first or perhaps the second version of IBM's controlled collapsed chip connection. This used a high melting point solder to create stand-off between the die and the substrate and used a low melting point solder for interconnection. The extra stand-off height generated by the high melting point solder made this interconnect more compliant than the typical solder bump found in most of today's flip-chip assemblies.

However in 1996, Xerox officially opened the door to this area of research by creating a true compliant interconnect as we now know it. This interconnect design harnessed the physics of magnetron sputtering to create curved compliant structures. By varying the chamber pressure during deposition of the moly-chrome alloy of which the interconnect was made, they were able to create a stress gradient within the deposited film. Upon patterning and release of these structures, the intrinsic stresses created within the thin films caused them to curl up to form free standing structures as shown in Figure 2-3. Since then a host of designs have been explored and characterized by several institutions. The rest of this chapter focuses on past and present technologies and gives and overview of the prominent designs available.

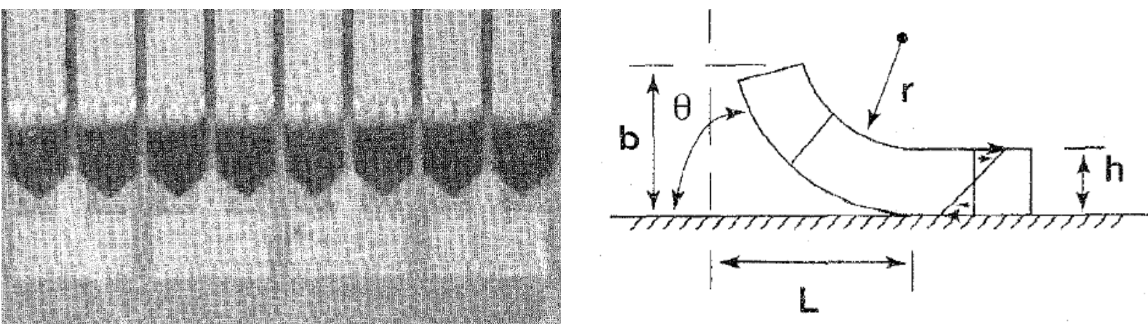


Figure 2-3: Xerox flip-chip technology for high-density packaging [24]

2.4. COMPLIANT INTERCONNECTIONS

The concept of utilizing compliant structures as interconnects has been around for over a decade. Several research groups with interest in the subject have created numerous designs each with unique characteristics. To streamline this discussion and for the sake of brevity, these interconnects have been sorted into three classes. These classes were selected based on their geometry and fabrication method. The three classes are: pillar designs, spring designs and 3D designs. The spring designs are also considered to be 3D structures, however owing to their higher compliance values and similarities in fabrication technique, it seemed reasonable to put them in a class of their own. The list of compliant interconnects reviewed in the following sections comprise of designs for either the 1st and/or 2nd level of interconnection.

2.4.1. Pillar Design Compliant Interconnects

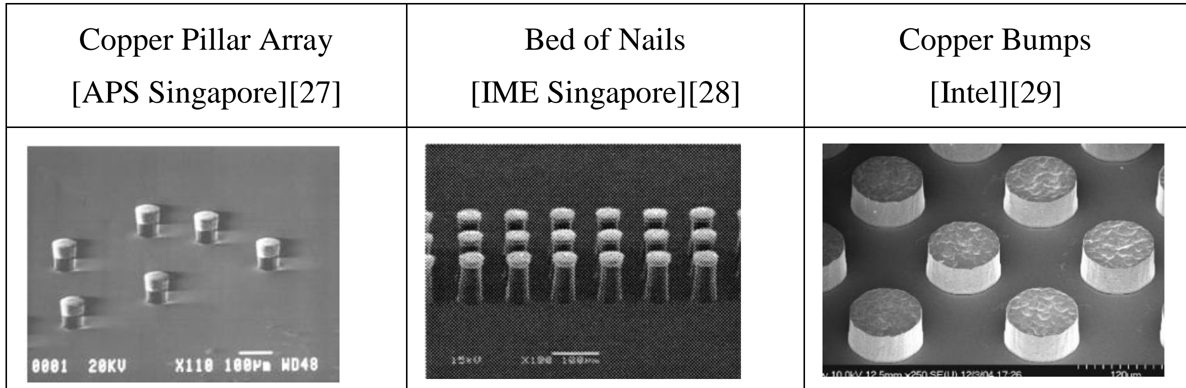
Pillar designs are a class of compliant interconnects based on a columnar design. These interconnects bear similarities to the first flip-chip packages produced by IBM. Their compliance is created by their higher stand-off height generated by the pillars/studs on which the solder is plated. The material of choice for most of these fabrications is copper which has a higher bulk modulus than solder. However, several publications on thin film electroplated copper all seem to show that the modulus of thin film electroplated copper could be lower than those of solder at room temperature. Modulus as low as 30 GPa have been reported by a number of researchers [25, 26]. Based on these findings,

the added compliance from the softer copper in addition to the increased stand-off height generated by the pillar improve the overall compliance of packages with this type of interconnect.

2.4.1.1. Pillar bumps

The first group of pillar based designs which include the copper pillar array [27], bed of nails [28], copper bumps [29] and the double ball structure [30] are conceptually simple and easy to realize. These leverage the solder bumping technique for their fabrication. The features are patterned over the pads and then the pillars are electroplated. Solder is then plated on the pillars for connectivity. Subsequently, the structures are released for assembly. While these interconnects are considered somewhat compliant, they are relatively stiff compared with true compliant interconnects and are likely to fatigue fail prematurely without underfilling.

Table 2-1: Copper pillars

Copper Pillar Array [APS Singapore][27]	Bed of Nails [IME Singapore][28]	Copper Bumps [Intel][29]
		

2.4.1.2. Polymer-Metal Hybrids

Interconnects in the second group employ polymers in their design to improve their thermo-mechanical reliability. Designs like the “low-κ compatible all-copper-flip-chip connections” and the “fine pitch metal-polymer core” interconnects employ polymers in their fabrication to relieve stress. The “all-copper” design uses a polymer collar to create a high aspect ratio copper pillar which is then electrolessly bonded to a substrate with a similar copper structure. The polymer collars increase the effective

diameter of the pillar in such a way that the highest strains in the assembly are experienced by the collars. The "polymer core" design on the other hand takes an inverse approach. High aspect ratio polymer collars are defined using an etch mask and plasma ashing process to etch out pillars from a thick layer of photoresist coating. The resulting structure is then electrolessly plated with copper to make it conductive. In this case, during thermal excursions from thermal cycling, the copper is exposed to higher deformation loads than its polymer core. However, since the structure is primarily composed of a polymer, it is much more compliant than a copper pillar of the similar dimensions.

The next three interconnects in this group namely, the Double ball structure, Super CSP and solder with polymer collar employ an encapsulating polymer at the base of the interconnect. These interconnects bear similarities with the first group of pillar designs with the exception of the encapsulant. Since these designs are not underfilled, the encapsulant is designed to relief the stresses at the base of the bumps/pillars thereby improving their reliability. The solder with polymer collar however is not a true compliant interconnect and may find application for non-low-κ assemblies such as second level interconnects.

The last interconnect design in the group is the plastic core solder ball. It bears striking similarities with the polymer core pillar by including a polymer at its core. The interconnect is created by electrolessly plating a thin layer of copper around the plastic core before solder is plated over the metalized structure. The copper keeps the solder on the core during reflow and assembly. The thinned conductive cross-section of this interconnect causes it to have a higher resistance than a traditional solder ball, but its compliance is derived through it. Like the polymer cored pillar, this interconnect moves the most stressed region away from the base of the interconnect and it has also been shown to have better reliability than solder. However, owing to its size, this interconnect may not find application as a first level interconnect.

Table 2-2: Polymer-Metal Hybrid Interconnects

Low-κ Compatible all copper flip-chip connections [31]	Fine Pitch Polymer Core interconnections [PRC][32]	Double Ball Structure [IZM][30]
Super CSP [Fujitsu][33]	Solder Interconnection with Polymer Collar [34]	Plastic core solder ball [35]

2.4.1.3. Nano-pillars

Another group of pillar based interconnects are the Nano-pillars. These are predominantly high aspect ratio pillars fabricated at the nano-scale range. As a result of their high aspect ratios, these interconnects tend to be very compliant. Based on the principles of mechanics, beam bending is the primary form of deformation that most compliant interconnects are subjected to. It can be shown mathematically that the smaller the cross-section of the interconnect, the lower the induced stresses in the structure for the same amount of displacement. Therefore if an interconnect height can be kept fixed and its cross-section significantly shrunk, it could potentially develop very little induced stresses during deformation. This is the basis for this group of pillar designs.

Table 2-3: Nano-pillar interconnects

Carbon nano-tube [NASA][36-38]	Z-axis compliant interconnects [25]	Multicopper-Column interconnects [39]
		15kV X800 20μm 0001 17 54 SEI

Carbon nano-tubes are perhaps one of the most explored materials owing to its unique properties. Its high thermal conductivity and electrical conductivity make it an idealistic compliant interconnect material. Researchers have been exploring its viability as a Level 0 and Level 1 interconnects. Their extreme aspect ratios make them very compliant. While their high aspect ratios make them an ideal solution for decoupling the die from the substrate, these structures have almost no mechanical strength. showed the modulus of forests of nanotubes to be in the range of a few Mega-Pascals [40]. This implies that assemblies employing CNTs as off-chip interconnects will need some form of die attach material to restrain the die from coming off the substrate. Perhaps a bigger challenge with the integration of CNTs will be their assembly. With a reported compliance on the order of about 10^3 mm/N for a CNT forest, these interconnects will deform at the slight pressure causing the interconnects to collapse on themselves [41]. Other issues include how to reliably connect CNTs electrically to exploit their superconductivity. Furthermore, not all CNTs are conducting upon deposition and may create assembly yield concerns [42].

As a result of these challenges with CNTs, researchers have developed an alternative approach to fabricating nano-scale pillars called the Z-axis interconnects. The fabrication used ceramic templates with nano-pores as mold to plate up nano-copper

pillars over the copper pads of both die and substrate. For assembly, the matching pads are flipped over each other and a compression force applied. Through a Velcro action the mating parts interlock. The limitation of this approach is the contact resistance that exists between the copper pillars. Also, it may be difficult to get the copper pillar forests to interpenetrate each other.

The Multicopper-Column interconnects share similarities with the Z-axis interconnects in fabrication processing and interconnect material. However, this interconnect uses conventional photolithography steps to create electroplating molds in photoresist. Hence while these have good aspect ratios compared to other pillar interconnects, they pale when compared with the CNT structures and the Z-axis interconnects. Another issue with high aspect ratio pillars is that they tend to have high self and mutual inductance and could contribute more to simultaneous switching noise [43].

In general, most pillar type interconnects have an advantage over other compliant interconnect designs in that they possess very desirable electrical characteristics such as low electrical resistance, inductance and perhaps capacitance depending on their footprint. A major drawback with this class of interconnects is their limited compliance. While more compliant than solder bumps, their limited compliance slightly improves their reliability for a no underfill application. Their low compliance values may not suffice in alleviating the stresses imposed on the die for large assemblies employing organic based substrates. Hence if a low-κ die is used with these interconnects, it could still result in a fracture or delamination of the low-κ material. The Nano-pillars on the other hand overcome the limited compliance with their slender design. However, the challenge of reliably integrating them as packaging solutions still remains.

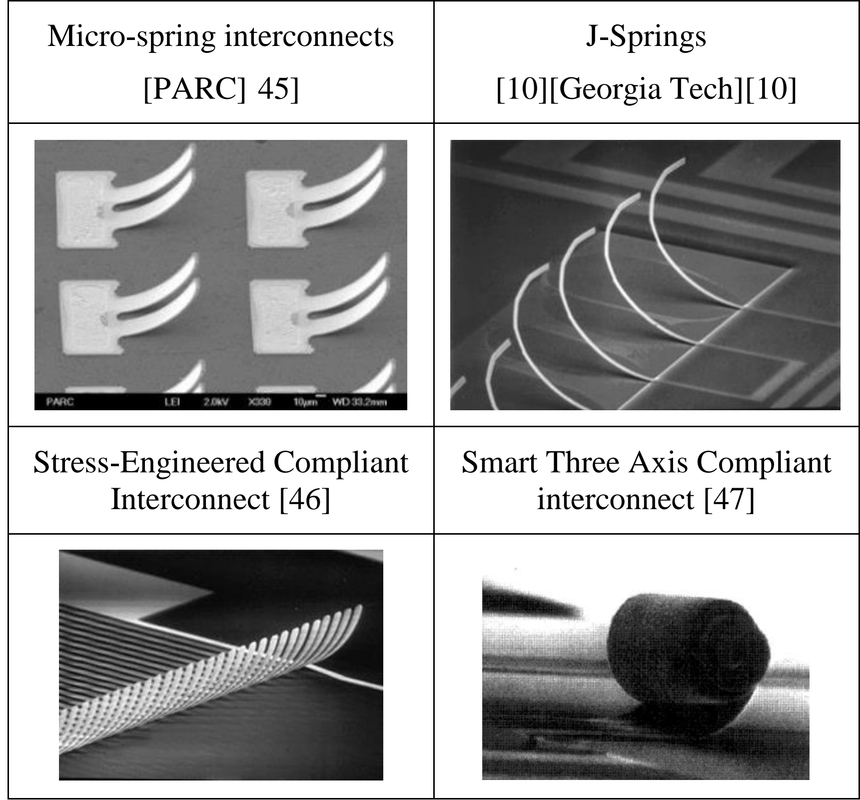
2.4.2. Intrinsically Strained Interconnects

Intrinsically strained interconnects derive their name from their method of fabrication. The principles employed in the development of this class of interconnect mimics the original compliant interconnect design proposed by Xerox.

The “Micro-Springs”, “J-Springs” and the “Stress-engineered” interconnects all use the procedure described for the Xerox design to create free-standing structures. Moly-Chrome is deposited with a continually increasing sputter chamber pressure to create a stress gradient in the deposited alloy. The stress gradient within the film varies by as much as -2 GPa at its base to 2 GPa on its surface [10, 44]. Upon patterning and release, these structures curl up to an equilibrium position giving rise to the free-standing structures in Table 2-4. A distinguishing difference between the “Micro-springs” and the others is that it has a gold coating intended to improve its conductivity and passivate the structure. The “Micro-spring” is also of a multi-path design which in addition to its gold coating helps lower its contact resistance and its overall resistance values.

Employing a different technique to create an intrinsically stress film is the “Smart Three Axis” interconnect. Unlike the other three designs in which a stress gradient is created in an exotic material to generate lift, this design uses a bimorph element to generate life/curvature. Two dissimilar metals with contrasting CTE’s are deposited on the wafer and then patterned. The high CTE metal such as copper is first deposited by electroplating, followed by sputtering of a thinner layer of low CTE metal such as tungsten. The wafer is then heated up to create a differential stress in the deposited films which leads to a curl of the film. To improve contact resistance, the interconnect is gold plated.

Table 2-4: Stress-released interconnects



Micro-spring interconnects [PARC] 45]	J-Springs [10][Georgia Tech][10]
Stress-Engineered Compliant Interconnect [46]	Smart Three Axis Compliant interconnect [47]

This group of interconnects is by far the most compliant of the three groups owing to their long slender nature. By design, most interconnects based on this approach do not use solder, but rather use simple contact to the substrate pad for assembly purposes. To hold such an assembly in place, an adhesive is used. A major drawback with this class of interconnects is that they have the highest resistance of most compliant interconnect types. The primary reason for the high resistance stems from the contact approach for electrical continuity between the interconnect and its mating substrate pad.

2.4.3. 3D Interconnects

This class of interconnects were named 3D Interconnects because their geometry is predominantly out-of-plane much unlike columnar interconnects that stand as towers. For example these interconnects cannot be modeled as 2D geometries as a 2D model will not be representative of the interconnect's true responses. These interconnects are

fabricated over some form of structural support which may or may not remain in the finished product. This is by far the most prevalent interconnect design class as several geometric designs are available. This class has been further sub-divided into groups based on their fabrication methodology/design. The first group, *Leads on Compliant Supports*, explores interconnects sitting on polymer/air cushions. The second group, *Serial Fabrication*, gives an overview of serially fabricated interconnects, while the third group, *Released Structures*, summarizes batch fabricated interconnects that are fully released.

This class of interconnects gain their compliance through out-of-plane components which allow their members to maximize their response to an applied load. Their compliance and electrical performance falls between those of the *Pillar Design Compliant Interconnects* and the Intrinsically Strained Interconnects. Depending on the design methodology, fabrication could be complex and expensive and in some cases not compatible with CMOS processing. A drawback with this class of interconnects is that they occupy more real estate than columnar interconnects because of their out-of-plane construct. While scalable, there is a limit to how small they can be scaled unlike the *Pillar Design Compliant Interconnects*.

2.4.3.1. Leads on Compliant Supports

Leads on Compliant Supports are a group of 3D interconnects with out-of-plane leads supported by compliant structures. The most elaborate designs captured in this group are General Electrics “Floating Pad Technology” and Tessera’s “Wide Area Vertical Expansion” interconnects. The GE design is based on a flexible Kapton tape on which photoresist is deposited, patterned and metallized to form the floating pad metal. The assembly is then inverted and vias are formed through the Kapton tape connecting the Floating pad on to the FPT metal on the backside. This assembly is then bumped and serves as a flexible interposer between the substrate and the board.

Table 2-5: Leads on Compliant Supports

Floating Pad Technology [GE][12]	Resin Core Posts [TI][29]	Bump on Flexible Lead [Fraunhofer IZM] [48]
ELAStec Wafer Level Packaging Technology [IZM][49]	Sea of Leads [Georgia Tech][50]	Wide Area Vertical Expansion [Tessera][51]

The "Wide Area Vertical Expansion" interconnects by Tessera also uses a polyimide based film for the fabrication of the interconnects. The flexible film consisting the interconnects were then bonded to the die matching the ends of the interconnects with the die pads. The assembly was then connected to an injection fixture through which a compliant polymer was injected between the polyimide film and the silicon die to create standoff and also serve as an encapsulant for the interconnects. Both fabrication methods are quite involved and could result in additional costs to the packaging process.

The "Resin Core Posts", "Bump on Flexible Lead" and "ELAStec Wafer Level Packaging Technology" on the other hand have the interconnects fabricated on the die over a compliant polymer base. This adds compliance to the bumps and a rotational degree of freedom to the bumped pads. The "ELAStec" method uses a raised compliant bump formed by printed silicone which improves the compliance of the structure over the

others. However, scaling of the ELAStec bump will be limited by the capabilities of the printing tool used. The fabrication process of these interconnects is relatively simple but the length of the leads can have an adverse effect on their electrical parasitics.

Lastly, the “Sea of Leads” compliant interconnect shares similarities with the ELAStec bump design. However, rather than using silicone injections to create bumps, it employs photolithography for the patterning of bumped regions. A thermally decomposable polymer is used to create bumps beneath the polymer overcoat and later decomposed to form air gaps beneath the overcoat. Vias are then formed through the overcoat through which the compliant structure is routed to the die pad. This interconnect suffers from the same limitations as the group, the long electrical leads can adversely affect their electrical performance.

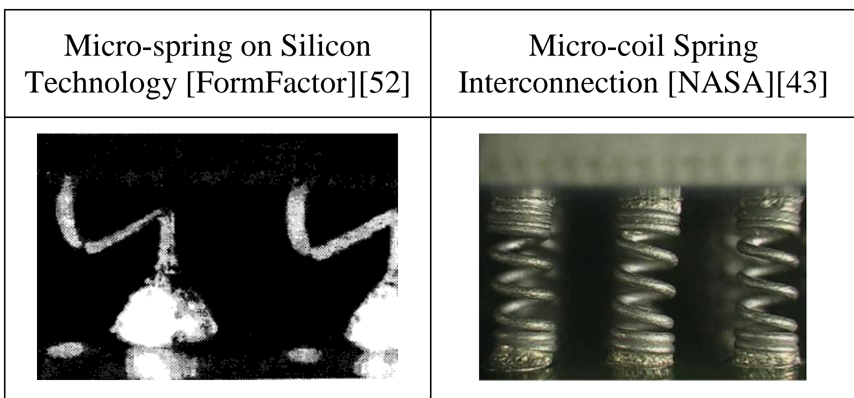
2.4.3.2. Serial Fabrication

The group of serially fabricated 3D interconnects utilize non-CMOS compatible processing to create the interconnects. The interconnects are serially fabricated directly or indirectly on the silicon wafer. Form Factors Micro-spring on Silicon Technology is one such interconnect fabricated directly on the wafer. The interconnect is formed through a wire-bonding process on the die pads of wafer. It is then coated with suitable metallurgy to provide spring properties. For very small dies and small scale operations, this packaging scheme may prove to be most economical as tooling for expensive photo masks and elaborate photolithography setups are not required.

The Micro-coil Spring developed by NASA on the other hand uses an actual spring made of beryllium copper as interconnects. The springs are coated with a 100 μin of electroplated eutectic tin lead solder to facilitate its assembly. While the fabrication process for the spring was not described, it can only be fabricated serially owing to its three dimensional nature.

Some foreseeable challenges with this group of interconnects include the sequential nature of their fabrication. This can result in higher costs for very large operations. Furthermore, these interconnects cannot not scale in pitch and can only be used as second level interconnects. As a result of their long electrical leads, their electrical parasitics may be too high for high performance applications.

Table 2-6: Serially Fabricated Interconnects

Micro-spring on Silicon Technology [FormFactor][52]	Micro-coil Spring Interconnection [NASA][43]
	

2.4.3.3. <u>Released Structures</u>

The third group of interconnects considered in the class of *3D Interconnects* are the fully *Released Structures.* These share similarities with *Leads on Compliant Supports* with the exception that all polymer layers and support structures are fully stripped at the end of the fabrication. The method of fabrication of these interconnects are very similar and a general description will be given.

Fabrication usually starts with the deposition of a copper seed layer, typically with a thin layer of titanium for adhesion purposes. Photoresist is then applied and patterned to generate posts for stand-off from the wafer or in the case of the “High-Density Compliant Die-Package” and the “Mechanically Flexible Interconnect” this resist layer is reflow to form a dome. To create the out-of-plane geometry, another seed layer is sputtered on the photoresist defining the stand-off of the interconnect before a second resist coating is applied in which the geometric designs defining the interconnect will be

electroplated. Lastly, solder is plated to the connecting ends of the interconnect in readiness for assembly.

For designs like the “G-Helix” and “Beta-Helix”, additional masking steps are required to be able to achieve the complete structure as illustrated in Table 2-7. Each additional masking layers has an additional associated cost that could make these designs, particularly the “Beta-Helix” expensive to implement. However, of all the designs listed in Table 2-7, it is the most compliant but at the expense of its electrical characteristics.

The dissimilarities among these interconnects is mostly geometrical. The “G-Helix” and “Beta-Helix” amongst this group are mostly likely to have the highest self-inductance based on their helical geometry. The “Flex connect” and the “Planar Micro-spring” are mostly likely to performed best electrically since both designs employ opposing current loops to send electrical signals to their pads. They are also of a multi-path nature which has been shown to have the potential to improve their compliance without adversely affecting their electrical resistance.

The “Mechanical Flexible Interconnect” based on its geometry is expected to have an impressive out-of-plane compliance but its in-plane response may be restricted. Of all the designs, the “High-Density Compliant Die-Package” is mostly likely to have the lowest compliance based on its structure as it appears to be a curved pillar interconnect. This assumption is supported by its need of underfilling to meet thermo-mechanical reliability requirements.

Overall, this sub-class of interconnects seem to hold a lot of promise as a potential solution to the low-κ dielectric assemblies. Owing to their out-of-plane construct however, there is a limit to how small these interconnects can be scaled in order to achieve ultra-fine pitches. In such a case, it would seem that the best packaging solution would use bumped pillars to connect the die to a low CTE interposer preferably silicon or glass with modified CTE to match silicon’s. In this scenario, the CTE mis-match would be removed from the first level interconnections thereby improving the thermo-

mechanical reliability of these joints. In such a case, the use of underfill will be unwarranted as the interconnects will remain predominantly stress-free through thermal cycling. With the underfill gone, the electrical parasitics of the interconnects at the first layer will be improved as the high-κ underfill material will then be replaced by air.

Table 2-7: 3D compliant structures

High-Density Compliant Die-Package [Intel][53]	Mechanically Flexible Interconnect [Georgia Tech] [11, 54]	Planar Microspring [Tessera][55]
Beta-Helix [Georgia Tech] [56]	G-Helix [57][Georgia Tech]	Flex Connect [14][Georgia Tech]

With the CTE mismatch now relocated to the second level which usually involves larger pitches than the first level, these compliant structures could then be applied as second level interconnects to create reliable assemblies. At the second level, these interconnects can easily meet the electrical requirements of high performance dies as a result of their large size. Nevertheless, for none performance intensive applications these interconnects designs will be able to meet the electrical requirements of first level interconnects.

Summary

- Interconnects such as Beta-helix employ a significant number of processing steps which translates to increased cost of implementation. In addition, the increased number of processing steps impacts yield adversely.
- Micro-spring interconnects tend to suffer from non-uniformity in the stand-off height based on stress variations across the wafer during material deposition.
- The out-of-plane interconnects and the micro-spring designs are characterized with high electrical parasitics. Examples include: beta-helix, micro-spring, J-springs, WAVE
- Designs such as Elastec WLP and SOL, which have their out-of-plane structures adhered to supporting domes, tend to have limited compliance.
- Some pillar-based designs such as copper bump need an underfill to achieve reliability target numbers and thus may not be suited for low–κ implementations.
- Almost all existing suites of compliant interconnects employ a single electrical path which could lead to a sudden device failure, if the electrical path fractures.
- With the exception of pillar-like interconnects and the beta-helix, most other designs have their die pad and substrate pad offset from each other. This creates additional design considerations, such as aligning the interconnects to the pads and orienting them in the direction of maximum in-plane strain.
- Interconnects such as micro-springs on silicon technology employing sequential wire-bonding-like fabrication are not wafer-level compatible and could lead to increased implementation cost. Owing to the limitations in the minimum wire diameter used in wire-bonding, and the pad area to make a bond, the micro-spring on silicon technology is not scalable.

CHAPTER 3

OBJECTIVES AND APPROACH

Having reviewed several compliant interconnect implementations, some of the drawbacks with these designs are explored to guide the development of an interconnect that perhaps will succeed in areas where other designs have failed. While it is understood that no one design can accomplish all set expectations, it is however possible to improve on existing interconnect designs to realize an interconnect solution with reasonable compromises to make them a feasible solution to the low-κ fracture problem.

3.1. GAPS WITH EXISTING SUITE OF COMPLIANT INTERCONNECT

This section gives an overview of the key areas where challenges still exist with current compliant interconnect designs and will be the areas of focus in the proposed design. The areas discussed include the cost of realization, the compliance of the interconnect, its electrical parasitics, its thermo-mechanical reliability and its ease of assembly.

3.1.1. Cost

The success of any product in today's competitive markets is heavily reliant on its cost. The best designs may have a hard time carrying through in the presence of lower cost yet effective solutions. With respect to compliant interconnects, low fabrication yields and several masking steps in fabrication can easily contribute to associated costs. Interconnect designs such as the Beta-Helix, Floating Pad Technology and Wide Area Vertical Expansion interconnects have elaborate fabrication processes that can greatly increase the cost of realization. Furthermore, the number of processing steps required to realize an interconnect structure exponentially increases the likelihood of fabrication defects which in turn translates to added costs. Designs such as the Wide Area Vertical Expansion interconnect, Plastic Core Solder ball, Carbon Nanotubes, Micro-coil Spring

interconnects and ELAStec Wafer Packaging Technology employ non-standard CMOS processing steps which can translate into additional equipment and processing cost.

3.1.2. Compliance

The importance of compliance stems directly from the ability of the interconnect to accommodate a certain amount of displacement with the generation of small reaction forces at its support. This phenomenon is very important in the design of compliant interconnects as the force transmitted through the interconnect could generate enough stresses to crack its low-κ dielectric support. While improved compliance over those of traditional solder bumps is welcomed, an overly compliant interconnect on the other creates assembly challenges and a susceptibility to vibrationally induced failures.

Interconnects such as pillar based designs i.e. copper bumps, copper pillar arrays, bed of nails to mention a few are only marginally more compliant than solder bumps. Muthukumar et al. mentioned that these interconnects have a 15-57% reduction in stresses [53]. This is a reasonable gain, however, depending on the size of the die, their compliance might not suffice as a larger die implementation is bound to significantly increase die stresses. Furthermore, because of the relative stiffness of these interconnects, they still require underfilling to prevent premature fatigue failures.

Overly compliant interconnects such as the Beta-Helix, Carbon Nanotubes, Micro-spring interconnects and stress engineered interconnects are some of the few interconnects with at least double digit compliance values. Which such high compliance, these interconnect designs are capable of literally decoupling die motions from those of the substrate's and in turn transmitting no forces across the assembly. While this yields the ideal expectation with in-plane motions, it also creates an unconstrained die effect in the out-of-plane direction. This implies that normal loading on the die perhaps from a vibrational shock load can accelerate the die off the assembly creating new reliability issues. Hence to be useful, overly compliant designs will require underfilling to restrain their out-of-plane degree of freedom to prevent catastrophic failures.

3.1.3. Electrical parasitics

The primary purpose of interconnects is to relay electrical signals to and fro the die and the system in which it is integrated. Therefore, the electrical parasitics of interconnects is of paramount importance in the efficacy of these interconnects in relaying signals. However, it is common knowledge that the premise of the field of compliant interconnects research and its primary objective (good electrical performance) are conflicting. To put this in perspective, an analogy will be drawn with respect to the field of structural optimization. The volume of a material and its structural strength go hand in hand. A larger diameter wire for instance can carry a larger load. But since weight is a function of volume, volume/strength cannot be increased without increasing weight. This condition also holds true for compliant interconnects. Compliance cannot be improved without degrading electrical performance for a given material set. Therefore, clever ways to approach this issue are needed. The field of structural optimization is one such field that created a work-around for this problem. Depending on the loading configuration and the geometry of the structures in design, stress analysis can be used to determine which regions on the structure support the largest loads and a material redistribution is performed until regions without any loading are eliminated and in effect reducing weight. While the solution of the structural approach is incompatible with compliant interconnect design which aims to improve compliance while maximizing volume, other physical phenomenon relating to stiffness and electrical conduction can be exploited to achieve a similar goal.

An important question then becomes "what is an acceptable value of parasitics for an interconnect?" There is no one answer that satisfies this question as each micro-processor design has its own unique performance requirements. For the purposes of this work, the ITRS forecasts will be used a guide in creating some basic expectations for the proposed interconnect design.

Looking over some existing interconnect designs, it will be observed that the most compliant species such as the Beta-Helix, Stress-engineered interconnects, J-springs have the highest electrical parasitics. The relatively long length of their conductors and their geometric layout are responsible for their increased parasitics. For instance, the helical nature of the Micro-Coil Springs developed by NASA makes it more of an inductor, and like an inductor, this interconnect design has one of the highest inductance values of interconnects with a similar pitch. The Stress-Engineered designs on the other hand, have relatively long traces in close proximity to other traces which can greatly increase capacitance and cross talk. In using multiple interconnects on a single pad such as CNTs, Z-axis interconnects, researchers have tried to address parasitic increases associated with increased compliance. These solutions however have other challenges that need to be addressed, such as conductivity and packaging issues in order to make them a viable option.

3.1.4. Thermo-mechanical reliability

While the conduction of electrical signals is the primary purpose of interconnects, the reliability of these conduits have become a very prominent factor in their design. A failed interconnect cannot transmit signals; hence, a structurally reliable interconnect solution is more desirable than an unreliable interconnect with perfect electrical characteristics. Interconnects based on the pillar design such as Copper Bumps and Copper Pillar arrays, have near idealistic electrical parasitics; however, these solutions are not the most reliable thermo-mechanically, as they are more likely to damage the ILD layers during reflow cool down due to their stiffness. During thermal cycling, these interconnects require underfill to achieve reliability targets but the presence of underfills increases the likelihood of ILD fracture. On the other hand, very compliant interconnects such as Micro-Springs and Stress-Engineered interconnects are so compliant that by themselves they cannot provide structural support. These interconnects also use require underfills in the form of adhesives which hold them die firmly against the substrate. By

contrast to these interconnect classes, very few Interconnects from the class of 3D Interconnects have shown reliability numbers. The lack of thermo-mechanical reliability numbers could stem from either of three causes: challenges with assembling these interconnects, low fabrication yield and defects, and perhaps less than desired thermo-mechanical reliability numbers.

3.1.5. Assembly

The assembly step completes the die packaging process. Only through assembly can a die be truly integrated into the rest of the system. Depending on the interconnect technology, assembly is carried out predominantly by reflowing solder to form electro-mechanical connections between the die and the substrate/board. Other options include the use of adhesives, both conducting and non-conducting to create electrical connections or to physically constrain the die to the substrate respectively. Newer methods of assembly include plating of materials such as copper across the pads to be joined in what is considered a low temperature bond process [31]. Another involves the use of nano-particles which lowers the bulk material’s melt temperature and in effect lowering assembly temperature [58]. A low assembly temperature reduces the damage incurred by the interconnects, since the effective strain is dependent on the range of thermal excursion.

To create a reliable and repeatable assembly process, these interconnects need to be rigid enough to support the weight of the die or measures can be put in place to achieve the same result. However, the use of additional structures to achieve mechanical rigidity or support could potentially increase assembly costs. For example, interconnect designs such as Micro-Springs [45] uses spacers to main the separation gap between the die and the substrate. The WAVE package on the other hand uses a custom adhesive injection process to create interconnect stand-off.

Lastly, interconnects belonging to the Pillar bumps subclass, for example, are plagued with white bump problems, particularly in large die implementations. As a result

of rigidity of these interconnects, excessive forces are generated at the interconnect/die interface during reflow cool down. These excessive forces typically result in the damage of the interlayer dielectric, and in effect, bring to an end a sample which takes several weeks to fabricate.

3.2. OBJECTIVES

Gaps identified with existing compliant interconnect designs was used as a starting point with the development of this interconnect solution. Key areas with identifiable challenges such as cost, compliance, electrical parasitics, thermo-mechanical reliability and ease of assembly of these interconnects were used as guides in the development of this interconnect. The objectives of this research are thus as follows:

- Develop a cost effective compliant interconnect solution. To be cost effective, this compliant interconnect leverages CMOS fabrication technologies which utilize standard tools currently available in most micro-electronic fabs. In addition to using standardized fabrication methodologies, the design is such that the least number of masking steps required to create the interconnects is used. In doing so, yield defects which tend to scale with the number of masking steps will be kept low and the added cost of additional process layers will be eliminated.
- Develop a reasonably compliant interconnect that will not crack or delaminate the low-κ ILD. A reasonably compliant solution should have enough compliance to accommodate the differential strain mismatch between the die and substrate without generating reaction forces at its support that are high enough to crack the supporting dielectric layers. Conversely, the interconnect will not be overly compliant such that assembly difficulties are created, and the rigidity of the assembled devices become compromised.

- Design the interconnects with reasonable electrical parasitics. The improvement of the electrical parasitics associated with on-chip interconnects led to development of low-κ dielectrics, which in turn is responsible for reliability failures of the ILDs. In addition to decoupling the die from the substrate, the compliant interconnects electrical parasitics should be such that its contribution to the RC delay does not exceed the contribution of the on-chip global traces.
- Develop a thermo-mechanically reliable interconnect solution that will be capable of enduring several hundreds of thermal cycles.
- Create an easy to assemble interconnect that will reliably survive the reflow cool down process of lead free solder. To be successful, the assembly process should be no more difficult than a solder bumped die assembly process.

3.3. APPROACH

To attain the set objectives, which are to create a low cost, easy to assembly and reliable interconnect with low electrical parasitics, projections based on the ITRS will be used as a guide to define feasible performance targets. Other standards such as JEDEC standards will be consulted for appropriate test setups that will yield results acceptable by peers.

From a cost perspective, the cost of fabrication will be kept low by using standardized CMOS fabrication processes in wafer batches. The fabrication sequence also hopes to minimize the number of masking steps required to create the interconnect. Earlier interconnects designs proffered by the group have good compliance values, but these can create assembly challenges and potentially other failure modes related to shock loading. To improve in this area, the compliance of the interconnect will be lowered to improve mechanical stability and boost electrical performance. To further improve on the electrical parasitics, a heterogeneous assembly of interconnects will also be explored. The

benefits of a heterogeneous assembly is improved overall current density and improved overall stiffness of the interconnects.

Lastly, a design of simulations approach will be used to study the impact of interconnects parameters on its thermo-mechanical reliability. This study will provide useful insights into which parameters to adjust to attain the desired reliability goal.

3.4. SCOPE OF RESEARCH

The scope of this research will be primarily focused on the development and fabrication of the multipath off-chip compliant interconnects. The work aims to demonstrate the feasibility of these interconnects by designing, fabricating, assembling and then testing these structures. Since the focus of the work will be on the interconnects, the fabrication sequence and models will not include wafer build-up layers nor standardized under-bump metallization. Through simulations, it will be shown that the interconnects are not only reliable but have been designed such that failure of the interconnect will occur within its arcuate structures. This implies that only minimal loads will be transferred to the adjoining solder bumps. Hence, failures related to solder will not be focused on, except in such instances where damage to the solder is used to determine its fatigue life for comparison with the interconnect structure.

Lastly, issues such as electromigration and the need for appropriate underbump metallizations to reduce or prevent electromigration will not be focused on as there are several publications on the subject, and the solutions to such problems can be easily adapted to the multipath fabrication process.

CHAPTER 4

DESIGN SELECTION

4.1. INTRODUCTION

Creating a successful compliant interconnect design is hinged upon understanding the behavior of these micro-structures and the challenge they are to overcome. As has been shown from the literature review, numerous compliant interconnect designs exist, some more compliant than others and others yet with more elaborate designs. As discussed earlier, several of these interconnects are inadequate in terms of meeting electrical, mechanical, fabrication, assembly, reliability, and other metrics. In this chapter, the design of proposed multi-path interconnects is presented taking into consideration the mechanical, electrical, and fabrication metrics.

4.1.1. Mechanical Compliance and Copper/Low-κ Dielectric Technology

The presence of pores in the low-κ dielectric greatly undermines their structural integrity. The pores aside from lowering the fracture strength of the material also act as stress raisers, which can amplify otherwise benign stresses to critical values further exacerbating the problem. Also, taking into consideration that low-κ dielectric materials have been known to have poor adhesion, the design of the compliant interconnects need to be such that it does not crack or delaminate the low-κ dielectric and thus, the interconnect needs to be compliant enough to avoid the build-up to critical stresses in the dielectrics.

4.1.2. Electrical Requirements

Other parameters of importance include the electrical properties of the interconnects. Since the interconnects function as channels for signal propagation across die and substrate, the electrical parasitics of interest are resistance, inductance and capacitance.

However the improvement of electrical parasitics typically compromises the mechanical compliance of the interconnect. Compliance by its very nature can be attained by lengthening the interconnect or by narrowing its cross-section. Both achieve similar results with respect to compliance, but could have a detrimental effect on the interconnect's electrical behavior. The electrical resistance is proportional to the length of the conductor but inversely proportional to the cross-sectional area of the conductor. Hence as described earlier, lengthening of the conductor or narrowing its cross-sectional area both act to increase electrical resistance. This means that any gain in compliance is offset by an increase in electrical resistance.

Several approaches can be used to address this compromise between the mechanical compliance and electrical parasitics. One approach is to employ multiple electrical paths within the same interconnect such that for the same mechanical compliance, the electrical resistance and inductance can be reduced. Such a parallel-path interconnect will use the concept of reducing overall mechanical stiffness of the interconnect by subdividing the area moment of inertias of the electrical path. Also, by appropriately selecting the current direction, the self-inductance of the interconnect can also be reduced. The second approach is to employ interconnects of varying geometry from the center to the edge of the die so that the mechanical compliance progressively increases toward the edge of the die where the differential displacement due to CTE mismatch is high. Such a varying geometry will have low electrical parasitics near the center of the die where such interconnects can be used for power and ground connections.

4.1.3. Process Steps and Cost

Regardless of the electrical and mechanical performance metrics, the cost of implementation is ultimately important for an interconnect to be commercially successful. Micro-machining technologies employing photolithographic processing are typically batch fabricated. The question of cost in such a scenario is narrowed down to the number of photolithographic steps required to fabricate the interconnect and the yield

of such a process. In this case, the number of masking steps becomes crucial, as fewer masking steps could result in significant cost savings and boost product yield as defect density increases with the number of masking steps.

4.2. DESIGN APPROACH

The approach used for the selection of the interconnect design in this work takes into consideration the parameters described above which are mechanical compliance, electrical parasitics and process steps. In an attempt to improve compliance while maintaining electrical resistance at a given value, a multi-path approach is employed.

Prior to discussing the proposed multi-path approach, it is helpful to discuss a parallel-path interconnect [59] where a single-path interconnect [60] (Figure 4-1a) is subdivided into two paths (Figure 4-1), as illustrated in Figure 4-1. The parallel path interconnect, as envisioned in Figure 4-1, has some limitations. One limitation is that the interconnect design has an overhang or cantilever approach from the die pad. Because of this overhang, the interconnect is likely to be susceptible to fracture under assembly forces. The second limitation is that the interconnect's die and substrate pads are laterally offset because of its overhang design. Such a lateral offset is inherently different from the traditional solder bump or ball interconnect where the die and substrate pads are aligned, and thus, the offset interconnect will not be an automatic plug-and-play replacement for solder bump interconnect. The third limitation is that the interconnect's planar compliance is dependent on the azimuthal angle, and therefore, the interconnect's orientation plays a role in obtaining the maximum planar compliance. Implementation of different orientations for the interconnects in the design layout is a challenging proposition.

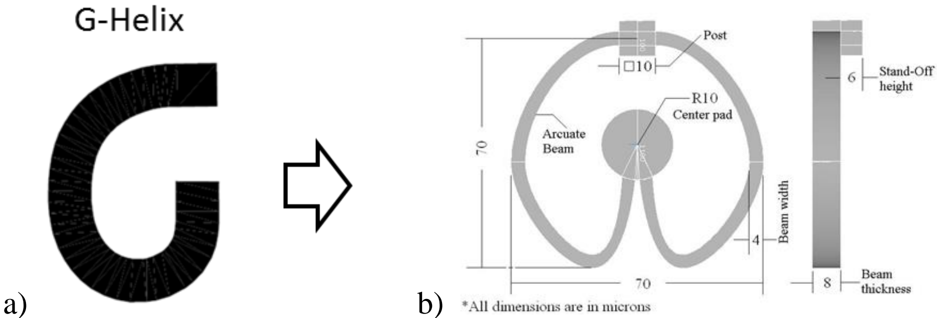


Figure 4-1: Flex Connect

As shown in Figure 4-2, revolving the original G-Helix design to generate more than two paths creates interference in the paths. To avoid this condition, the paths are shortened such that they can be accommodated within a circle. Likewise, with a fourth degree multi-path design, the paths would need to be shortened even further to prevent interference.

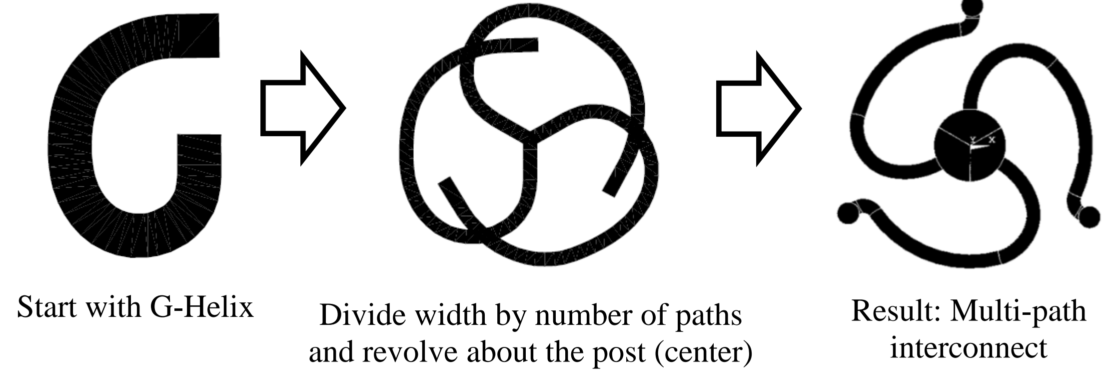


Figure 4-2: Evolution of the multi-path interconnects from G-Helix

4.3. MULTI-PATH COMPLIANT INTERCONNECTS

Besides the actual values of electrical parasitics and mechanical compliance, keeping in perspective the other requirements associated with multi-path compliant interconnects such as aligned die and substrate pads, directional independence of planar compliance, acceptable number of processing steps, etc., several multi-path interconnect designs were explored. As the die and substrate pads are aligned, one way to achieve in-

plane compliance is to employ parallel path structures that have planar shapes defined by polynomials. For a given number of parallel paths, as one would anticipate, as the order of the polynomial for each path increases, the planar compliance value also increases, and also the electrical parasitics. Also, higher order polynomials create several sharp radii to accommodate the annular gap between the die pad and the substrate pad. Also, fabrication of higher-order polynomial arcuate structure is difficult given the aspect ratio limitations associated with different photoresist materials. On the other hand, straight radial lines connecting the substrate pad to the die pad do not provide enough planar compliance. In this work, a third-order polynomial curve is used to represent the arcuate structures so as to provide enough compliance as well as facilitate easy fabrication.

To understand multi-path interconnects better, three (3) variants were explored: a two-path, a three-path and a four-path design. Figure 4-3 illustrates the basic layouts of each of these variants. It should be emphasized that these three designs are exploratory designs and only serve to compare the capabilities of the three designs being explored. The essence of this current chapter is to gain a general understanding of the behavior of these three designs from which one can be selected for further study.

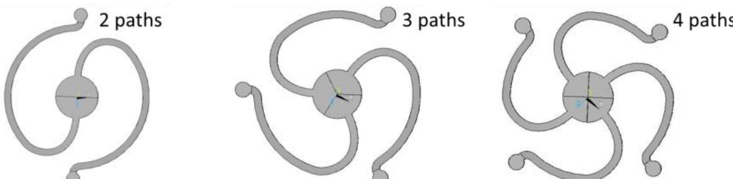


Figure 4-3: Base design of the 2, 3 and 4 path interconnects

Through the initial design process, only one multi-path compliant interconnect design is to be selected for further study. To do so, test parameters to contrast the capabilities of each of the designs were needed. For this preliminary study, the factors of interest included the compliance of the interconnects and their electrical parasitics. This study starts with an interconnect with a single arcuate beam whose dimensions are 8 µm x 8 µm square cross-section. These initial dimensions are consistent with the dimensions

used for single-path G-Helix [57] that has been optimized for electrical and mechanical compliance.

When designing and fabricating the multi-path interconnects, several factors were taken into consideration. The length and the cross-sectional area of the arcuate beams define the electrical resistance of the interconnect, while the length, shape, orientation, and cross-section of the arcuate beams define the inductance of the interconnect. The compliance of the interconnect is influenced by the length of the arcuate beam as well as the area moment of inertia along two orthogonal directions. Thus, it is nearly impossible to keep all of these parameters the same across the three different designs in an attempt to create a common basis of comparison amongst them. Thus, as a first approximation, the total area of cross-section was kept the same for the three interconnect designs under consideration. The length of the interconnects, on the other hand, is governed by the annular distance between the outer annulus and the inner pad, and thus difficult to ensure that the total length of all arcuate structures will remain the same. It is also important to ensure that the cross-section can be easily fabricated. Based on photolithography limitations, the width of the arcuate structures will not be less than 4 µm. Thus, to keep the total cross-section area the same for all three interconnects, the width and the thickness of each arcuate beam in a two-path interconnect were 4 µm and 8 µm, respectively; the width and thickness of each arcuate beam in a three-path interconnect were 4 µm and 5.3 µm, respectively while the width and thickness of each arcuate beam in a four-path interconnect were 4 µm and 4 µm, respectively. The dimensions of each of the designs are listed in Table 4-1. Figure 4-4 embodies the features dimensioned in Table 4-1.

Table 4-1: Simulation parameters of 2, 3 and 4 path interconnects

Dimensions [μm]	2-path	3-path	4-path
Width	4	4	4
Thickness	8	5.3	4
Stand-off	9	9	9
Center pad rad	10	10	10
Area[μm^2] (path)	32	21.2	16
Area[μm^2] (total)	64	63.6	64
Path length	106	75	59
Footprint	76	76	76

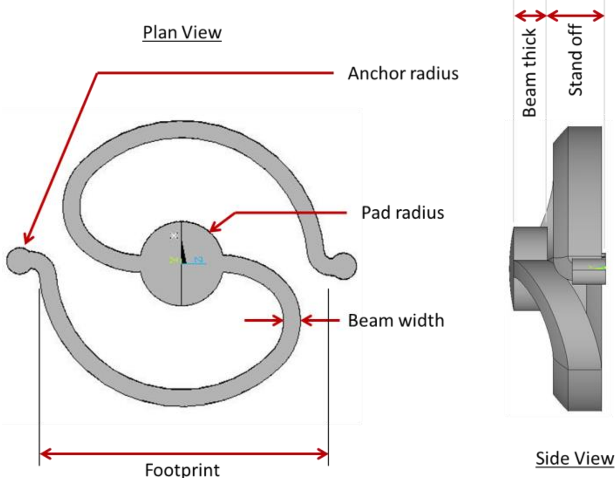


Figure 4-4: Description of interconnect's features

Several simulations were performed to determine the characteristics of each of these interconnect designs. The simulations performed include numerical modeling for the determination of resistance, inductance and compliance of the interconnects. The setups for these simulations including the applied boundary conditions are discussed in Chapter 5. The results of the simulations are listed in Table 4-2 to aid in the comparison and selection of the interconnect design best suited for further study.

Table 4-2: Mechanical and Electrical performance of 2, 3 and 4 path interconnects

	2 path	3 path	4 path
Electrical simulations			
Resistance [mΩ]	31.1	22.1	17.4
Inductance [pH]	69.8	43.4	24.9
Mechanical simulations			
Compliance [mm/N]	2.2/5.6*	1.09	0.602
Out-of-plane	4.75	2.48	1.67
Orientation dependent	Yes	No	No
Fatigue Life [cycles]	3195	308	166
Strain range	0.00279	0.0117	0.0165

Based on the conductor (path) lengths listed in Table 4-1 and given that each design has same total cross-sectional area, it was expected that the designs with shorter conductor lengths would have lower resistance and is validated by resistance simulation results shown in Table 4-2. The inductance of the interconnects follow a similar trend, interconnects with shorter conduction paths have lower self-inductance than variants with longer paths. However, unlike the electrical resistance, which varies linearly with the length of the conductor, the inductance values tend to deviate from this linear dependence. For example, the resistance increase between a two path interconnect and four path interconnects is roughly 79% which is the same as the increase in conductor length. However, with respect to the increase in inductance, the two paths' is 180% greater than the four paths'. This is because inductance is dependent on the radius of curvature of the arcuate structure, number and direction of electrical paths, as well as the arcuate structure length and cross-section.

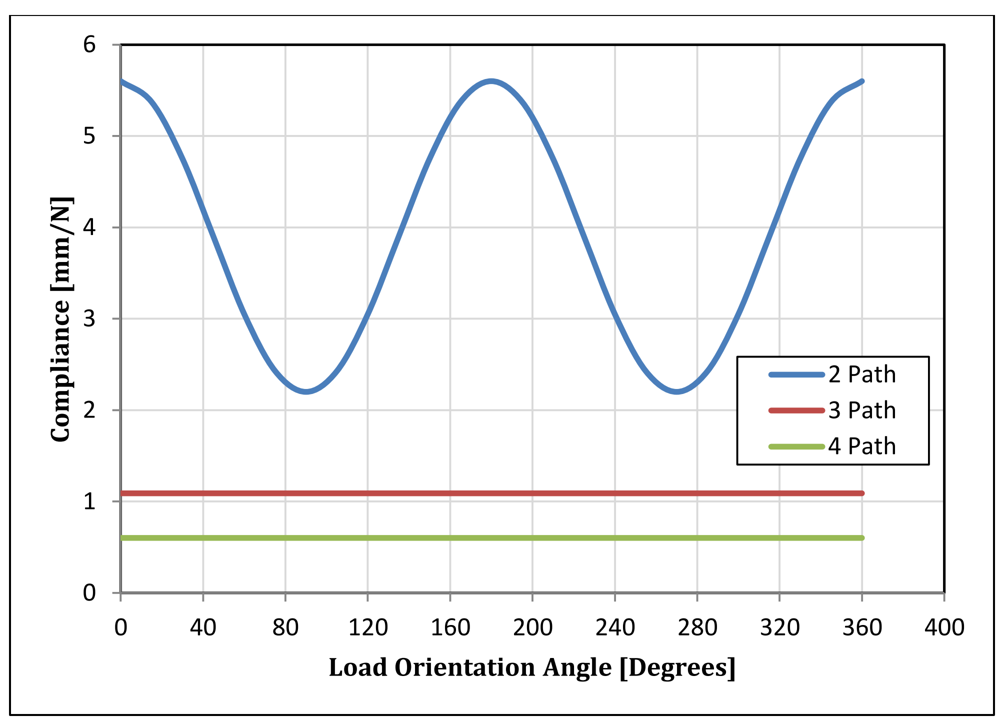


Figure 4-5: 2, 3 and 4 Path Interconnect's compliance response to variable orientation in-plane loading

For the mechanical responses of the interconnects, the simulations of both in-plane and out-of-plane compliance also followed a trend related to the interconnect's path lengths. The two path design with its longer path lengths out-performs the others both in in-plane and out-of-plane compliance. However, much like the trend in inductance, these values deviate from the ratios of the path lengths. This is as a result of the cross-sectional area of the beams. The 3 interconnects have different beam cross-sections, therefore making their second moment of area, which is cubically dependent on one of the cross-sectional dimensions, different.

The in-plane compliance simulations were then taken one step further to assess the stability of these structures. Simulations of in-plane compliance as a function of load orientations were conducted for each of the three interconnect designs. The objective of this test was to determine if multi-path interconnects had directionally dependent compliance. Figure 4-5 is a plot of the outcome and it shows that the two path design has in-plane compliance that is strongly a function of the orientation of the applied load. The

higher order paths show little-to-no-dependence on load orientation. This implies that the three and four path designs are more stable and will have a more predictable response to an applied load.

Based on the above electrical and mechanical metrics, it is clear that the three-path interconnect will provide intermediate values for both metrics, and at the same time, will provide in-plane compliance that is not dependent on the orientation of the interconnect. The discussion, presented thus far, is largely applicable to different pitches of two-path, three-path, and four-path interconnects with appropriate dimensional scaling.

CHAPTER 5

MECHANICAL AND ELECTRICAL MODELING METHODOLOGY

5.1. INTRODUCTION

Having selected three-path interconnect as a viable compliant interconnect based on its electrical and mechanical compliance metrics, this chapter provides more details on the modeling methodology employed. As the focus of this thesis is more on the mechanical compliance, thermo-mechanical deformation, and thermo-mechanical reliability, than on electrical parasitics, the discussion is appropriately scaled in the following sections.

5.2. MATERIAL MODELING

Constitutive behavior of materials plays an important role in understanding the response of the interconnect structure to the applied load. Depending on the range and type of load applied, the constitutive behavior will be simply linear, temperature-dependent linear, bi-linear, or non-linear. Also, it could be time-dependent as in viscoelastic or viscoplastic deformation. This sub-section lists the material properties used for all modeling tasks in this work. The materials include: copper which is capable of predicting material non-linearities such as plasticity, lead-free solder which also incorporates time dependent non-linearities such as viscoplasticity and material models for the silicon die and FR4 board which were modeled as simple temperature- and direction-dependent elastic materials, as appropriate.

5.2.1. Copper

The copper model used was a kinematic hardening isotropic material model. Ductile materials such as copper exhibit strain hardening so a kinematic hardening model was used to describe its behavior [61, 62]. To capture the effects of plasticity and yielding, the material model includes a stress-strain response which defines the yield point and the plastic response of the material and is plotted as Figure 5-1. For increased

accuracy, the material model also incorporates temperature dependency. As seen in Figure 1, copper behavior is not highly dependent on the temperature of interest – room temperature to reflow temperature. In general, the modulus based on the slope of its response at room temperature is 121 GPa with a yield strength of 121 MPa. The resistivity value used was 1.77e-8 Ωm.

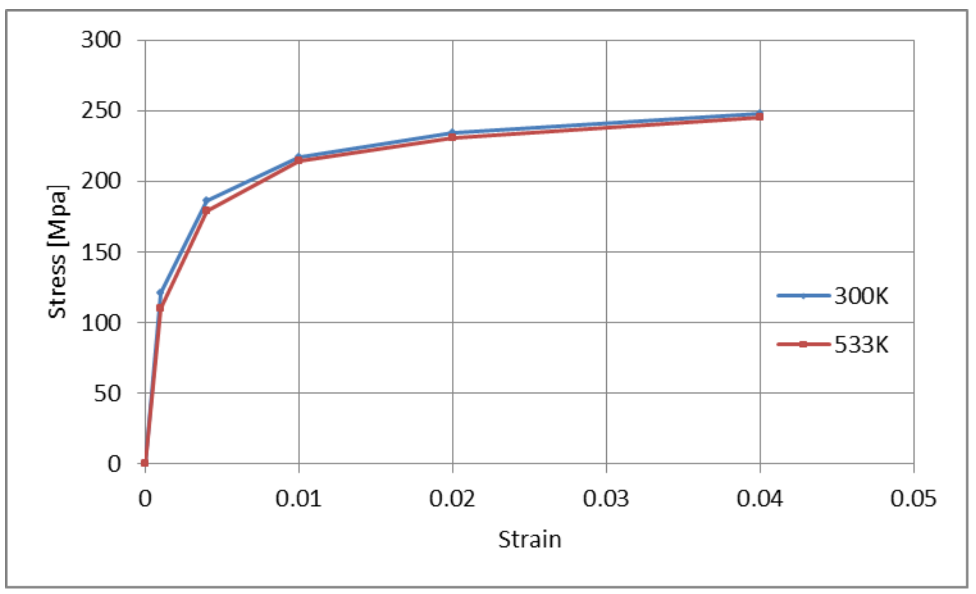


Figure 5-1: Stress-strain response of modeled copper behavior at 2 different temperatures

5.2.2. Solder

Solder at room temperature is a viscoplastic material. This implies that if subjected to a static load for a duration of time, that the material will creep in the direction of the load. Upon removal of the load, there is usually very little elastic recovery and the material holds its deformed profile. To capture the time and temperature dependent effects of creep in the material model, Anand's model for viscoplasticity was used to model the behavior of the tin-silver (Sn3.5Ag) alloy used in assembly. The parameters used in the model are listed below. The equation describing Anand's viscoplastic model is given in Equation 1.

$$\frac{d\varepsilon_p}{dt} = Ae^{(-Q/RT)}\left[sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}}$$

Where $$\dot{s} = \left\{signh_o\left|1 - \frac{s_o}{\hat{s}}\right|^a\right\}.\dot{\varepsilon}_p$$

And $$\hat{s} = \hat{s}\left[\frac{\dot{\varepsilon}_p}{A}e^{(Q/RT)}\right]^n$$

Equation 1: Anand's model for viscoplasticity [ANSYS]

Mechanical properties		
Young's Modulus	E	49.2 MPa
Coefficient of thermal expansion	α	24 ppm/K
Poisson's ratio	ν	0.4
Electrical properties		
Electrical resistivity	ρ	77.8 nΩ/m
Anand's parameters		
Initial value of deformation resistance	s_o	39.09 MPa
Activation Energy/Universal gas const.	Q/R	8900 K^{-1}
Pre-exponential factor	A	22300
multiplier of stress	ξ	6
strain rate sensitivity of stress	m	0.182
hardening/softening constant	h_o	3321.2 MPa
coefficient for deformation resistance saturation	ŝ	73.81 MPa
strain rate sensitivity of saturation	n	0.018
strain rate sensitivity of hardening or softening	a	1.82

5.2.3. FR4

5.2.3.1. Mechanical

Owing to the physical size and thickness of the substrates compared with the interconnects in the models, FR4 was modeled as a temperature dependent linear elastic orthotropic material. To further simply modeling efforts and to ease computational resource requirements, a smear model of the substrate was used in the place of a composite board comprised of several members as illustrated in Figure 5-2.

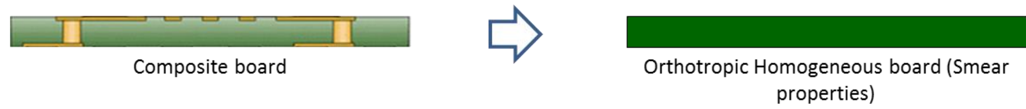


Figure 5-2: Simplification of board composition/properties

Mechanical properties (Smeared)		
Modulus*	E_x, E_z (E_y)	22.4(1.6) GPa
CTE*	α_x, α_z (α_y)	11(25) ppm/K

* Properties below glass transition temperature of 180 C (Out-of-plane)

5.2.3.2. Electrical

The electrical properties of the board used for high-frequency simulations came from the manufacturers literature of the product used. The laminate type used for the fabrication of the test vehicle was Isola IS410 having the general properties listed below.

Electrical properties @ 1GHz	
Relative Permittivity	3.9
Loss Tangent	0.0189

5.2.4. Silicon

Silicon was modeled as a temperature-dependent linear elastic isotropic material with a modulus of ~120 GPa at room temperature. The properties used represent the properties along the length of the modeled strip in the direction of the neutral point of the die, and should give reasonably accurate results for the simulations performed. The CTE of silicon used was 2.6 ppm/K.

5.3. MECHANICAL COMPLIANCE SIMULATION

Compliance characterizations of the interconnects were performed for both the in-plane and out-of-plane directions. The in-plane compliance mostly determines the ability of the interconnect to decouple the lateral motion between the die and the substrate. The out-of-plane compliance, on the other hand, helps the interconnects adjust to surface non-planarities of the substrate or other mating surface mostly resulting from substrate fabrication and thermally-induced warpage.

Figure 5-3a and b illustrate the setups used in the compliance simulations. For the out-of-plane compliance, the base of the interconnects were constrained in all available degrees of freedom representing the actual boundary conditions of the fabricated interconnects. A 1 mN force was then applied vertically downward (in the out-of-plane direction) on the center pad as indicated by the force arrow in 3a. The corresponding displacement at the point of equilibrium in the direction of the applied load was extracted and divided by the applied load to give the out-of-plane compliance.

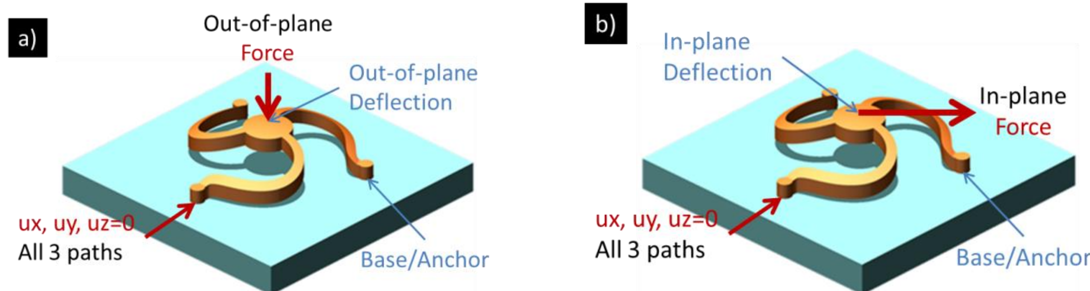


Figure 5-3: Finite element setups for (a) out-of-plane compliance (b) in-plane compliance

A similar approach was used for the in-plane compliance determination. The difference in this case is in the orientation of the applied force. The force is applied in the plane of the wafer i.e. parallel to the surface of the die. The corresponding in-plane displacement in the direction of the applied force is then obtained and divided by the applied force to obtain the in-plane compliance.

To measure the dependence of the in-plane compliance of the interconnects on the direction/orientation of the applied force, the model was updated with a variable direction load force as shown in Figure 5-4. The interconnects were constrained as before and the variable direction force was applied at different angles in 10 degree increments for a total of 360 degrees. The compliance was then obtained by extracting the displacements in the direction of the force and dividing by the magnitude of the force.

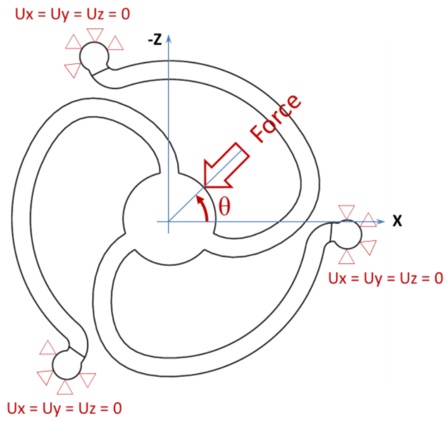


Figure 5-4: In-plane compliance simulation setup

5.4. THERMO-MECHANICAL STRESS/STRAIN MODELING

Perhaps the most critical of the characterization tests of the interconnect is its thermo-mechanical reliability as this gives a measure of the useful life of the interconnects when in service. Given the dimensions of the assembly listed in Chapter 4, a full model of the assembly would appear as depicted in the Figure 5-5. As seen, the assembly will consist of a silicon die, an array of interconnects, and the organic substrate.

Considering that the interconnects are micro-scale structures assembled onto component parts (die/substrate) whose dimensions are several orders of magnitude greater, the computational resources needed to solve such a problem would be immense and could take several days to solve.

To ease the computational requirement needs to simulate the assembly, a strip model highlighted in white in the left image of Figure 5-5 was extracted from the full assembly. The right image of Figure 5-5 highlights the cross-section of the modeled strip. The Strip model, also known as a generalized plane displacement (GPD) model greatly reduces the number of interconnects needed to be modeled whilst retaining good accuracy. A strip model is a reduced 3D model that contains one row of interconnects as well as the die and the substrate. The width of the strip model is equal to the pitch of the interconnect so that the model contains at least one row of interconnects with gaps on both sides. The strip model preserves the 3D geometry of the interconnect, unlike a 2D plane model which will not be able to represent the 3D nature of the interconnect. At the same time, a strip model is computationally less expensive than a full-blown 3D model, as the full-blown 3D model will need to account for all interconnects in the assembly, taking into consideration appropriate symmetry conditions.

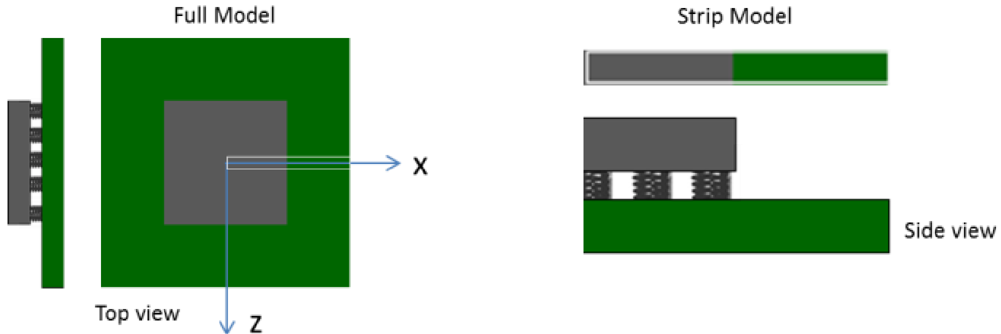


Figure 5-5: Left image is a picture of the full assembly. Right image is a cut-out strip (highlighted in white in left image) representing the portion of the assembly modeled for thermo-mechanical reliability assessment.

The boundary conditions applied to the strip model and illustrated in Figure 5-6 are as follows: on the parallel sliced faces, z faces, nodes are coupled such that nodes on individual material structures (silicon die or organic substrate) expand or contract by the same amount. Symmetry boundary conditions along x axis are applied at the rear cut end of the strip while a single node at the bottom of the substrate is constrained in all degrees of freedom to prevent rigid body motion.

Since the silicon die with interconnects is assembled on organic substrate through solder reflow, the structures are assumed to be stress-free at the melting temperature of solder. For a eutectic tin-silver (Sn3.5Ag) solder, the melting point is 221 ^{o}C. As the assembly is cooled from this stress-free melting temperature, the die and substrate become mechanically coupled through the interconnects and the solidifying solder. The coupling of the die to the substrate with mismatched CTEs commences the buildup of stresses in the assembly as the assembly is cooled. Upon attaining room temperature conditions, the induced stresses and strains in the assembly can be obtained. The warpage of the assembly and residual stresses in the die upon assembly and cooling to room temperature can also be obtained.

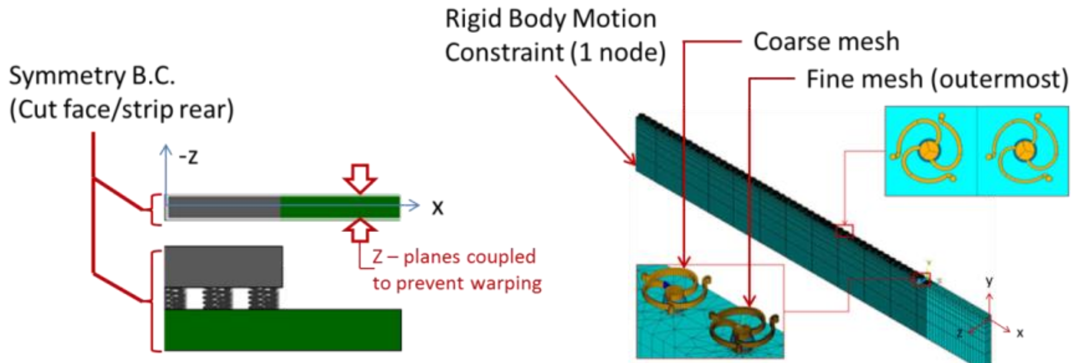


Figure 5-6: Generalized plane displacement model of a strip from the Interposer assembly. Interposer is hidden in right image to reveal interconnects

After the reflow process is simulated, the assembly is then subjected to thermal cycling loads as outlined in JEDEC standard. In this work, the assemblies were

simulated to be subjected to 0 to 100 ^{o}C at 50 minutes per cycles with a ramp rate of 5 ^{o}C /min and a dwell duration of 5 minutes at the hot and cold temperatures. Table 5-1 lists the criteria for thermal cycling between the temperature limits of 0 and 100 ^{o}C based on JEDEC JESD22's temperature cycling standard.

Table 5-1: Highlights of JEDEC JESD-A104D type J [63]

	low	high
Temperature cycle [^{o}C]	0 (+0, -10)	+100 (+15, -0)
Cycle rate [cph]	1	3
Soak [mins]	-	5
Ramp rate [^{o}C/min]	10	15

5.4.1. Thermal Cycling Fatigue Life Predictive Modeling

5.4.1.1. Failure Metric

The thermo-mechanical reliability requirements for the fatigue life of most microelectronic devices falls within the low cycle fatigue regime of less than 10,000 cycles to failure. Within the low cycle regime, Coffin-Manson-based equations employing strain range ($\Delta\varepsilon_p$) as a failure metric are typically used to predict fatigue life. Equation 1 shows a generic Coffin-Manson equation and the coefficients a and b are material dependent parameters. N_f represents the fatigue life to failure and ε_f the ductility coefficient which ranges between 0.15 and 0.3 for copper [64]. The total strain the material undergoes during plastic deformation is a linear combination of the recoverable elastic strains and the dissipative plastic strains as shown in Equation 2.

$$\varepsilon_{total} = \varepsilon_{elastic} + \varepsilon_{plastic}$$

Equation 2: Total strain as a summation of elastic and plastic strain

Since the elastic strains are recoverable, it can be assumed that deformation within the elastic range leads to an infinite life. Subsequently for the assessment of low cycle fatigue, the parameter of interest is the plastic strain. Figure 5-7 depicts the hysteresis loop for a typical ductile material undergoing cyclic deformation. As this image shows, the plastic strain ($\Delta\varepsilon_p$) dominates in the low cycle regime. The plastic strain amplitude which is the failure metric used is computed over the stabilized hysteresis loop and substituted into the Coffin-Manson equation to estimate the fatigue life. The hysteresis loop is considered stabilized when it forms a closed loop and the stress-strain path in subsequent cycles does not change. The expression for computing the equivalent plastic strain for each load-step is shown in equation 3. The accumulated plastic strain over one complete cycle is obtained by using strain tensor component increments through each load step. For the simulations performed, the hysteresis loops stabilized after the third thermal cycle, and the accumulated plastic strain range from this loop was used as an input to compute the thermo-mechanical fatigue life.

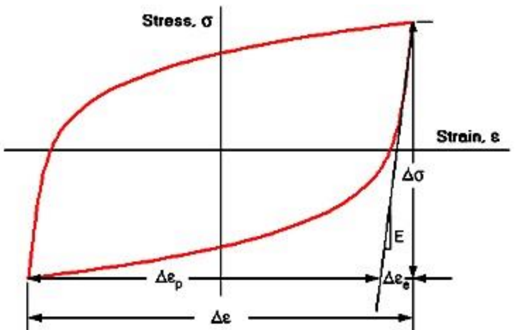


Figure 5-7: Hysteresis loop for ductile material

Figure 5-8 shows the thermal profile associated with assembly cool down and subsequent thermal cycling of flip-chip assemblies with compliant interconnects.

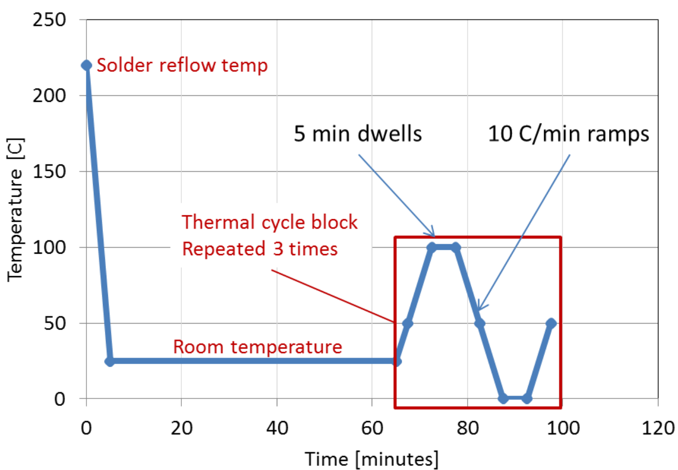


Figure 5-8: Temperature cycle profile used in thermo-mechanical simulations

$$\varepsilon^{p} = \sqrt{\frac{2}{3}\varepsilon_{ij}^{p}\varepsilon_{ij}^{p}}$$

Equation 3: Tensor representation of equivalent plastic strain

5.4.1.2. <u>Thermal Cycling Fatigue Life</u>

Once the equivalent plastic strain range from the stabilized cycle is computed, it can be used to determine the thermal cycling fatigue life of the compliant interconnects. The two possible locations where the interconnect could fatigue fail are the copper interconnects themselves or the solder joints which are used to attach the interconnect to the substrate. As both structures are low-cycle fatigued, meaning that the number of thermal cycles is a few thousands at best, a strain-based damage metric will be used as discussed in the previous section.

Based on Engelmaier's work on the round robin study for IPC copper foils [65], equations to predict the fatigue life of thin sheets of copper was reported based on the total strain. Total strain was used because this is an observable quantity. However, the expression based on the total strain of copper is an implicit function of the fatigue life being calculated as described in Equation 4.

$$N_f^{-0.6}\varepsilon_f^{0.75} + 0.9\frac{S_u}{E}\left[\frac{e^{\varepsilon_f}}{0.36}\right]^{0.1758 log10^5/N_f} = \Delta\varepsilon$$

Equation 4: Total strain based fatigue life prediction model

The implicit nature of the equation makes the automated computation of fatigue life cumbersome. However, a second expression which is a simplification of Equation 4 uses only the plastic strains (a derived quantity) as an input to calculate fatigue life. In doing so, the equation for fatigue life is greatly simplified to the explicit equation listed as Equation 5.

$$N_f^a \varepsilon_f^b = \Delta\varepsilon_p$$

Equation 5: Plastic strain based fatigue life prediction model

However, it should be pointed out that the Simplification of Equation 4 to yield a simpler expression will introduce inaccuracies in fatigue life predictions. Iannuzzelli reports that the inaccuracies are conservative and can under predict fatigue life cycles by as much as 20% depending on the proximity of the results to the applicable range [66].

For the prediction of solder fatigue life, the Coffin-Manson based equation listed as Equation 6 is used. N_f is the mean number of cycles to failure, C and m are numerical constants and the values used for Sn3.5Ag were $C = 21.9$ and $m = 0.93$ [67].

$$N_f = \left[\frac{C}{\Delta\varepsilon_p}\right]^{\frac{1}{m}}$$

Equation 6: Coffin-Manson equation for tin-silver fatigue life prediction

5.5. ELECTRICAL SIMULATIONS

Several electrical modeling tools were used to simulate the various parameters of interest. In other cases, one tool was used as a check for another to ensure consistency in results. The tools used for electrical simulations include: ANSYS, Ansoft Q3D, FastHenry and Ansoft HFSS.

5.5.1. Electrical Resistance

The electrical resistance of the interconnect was first determined through ANSYS. The setup is as illustrated in Figure 5-9. Much like a four wire measurement, a current of 1 mA was applied at the center pad of the interconnect. The base of the interconnect was then grounded to zero potential. The potential drop across the center pad and ground was then extracted and divided by the applied current to obtain resistance. This was verified through hand calculations and provided the basis to check the outputs of other models.

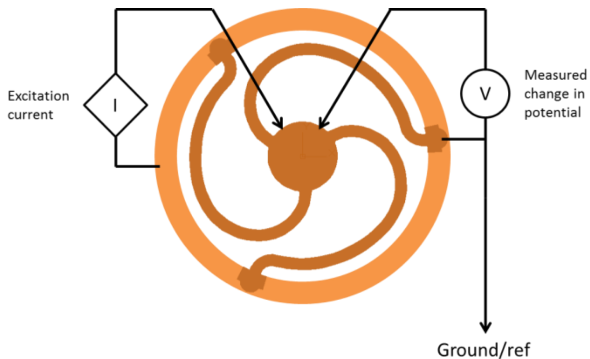


Figure 5-9: ANSYS resistance measurement setup

For the analytical model of the interconnect coupled with its annular die pad, a complex resistor network is formed. This complex resistor network was then converted into simple lumped resistors connected by lossless wires, as shown in Figure 5-10. The inlets and outlets of the resistor networks were then identified to define the current paths. Then using Kirchoff's current law the matrix representation of Ohm's law was derived for the network and solved for the influx current, i_4. Dividing the source voltage V, by the total current i_4, the effective resistance of the network was obtained.

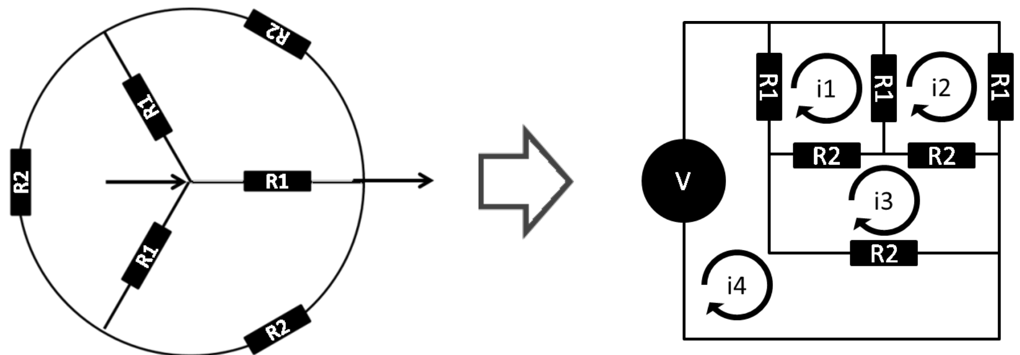


Figure 5-10: Representation of resistor network for analytical calculation

$$\begin{bmatrix} R1+R1+R2 & -R1 & -R2 & -R1 \\ -R1 & R1+R1+R2 & -R2 & 0 \\ -R2 & -R2 & R2+R2+R2 & -R2 \\ -R1 & 0 & -R2 & R2+R1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ V \end{bmatrix}$$

Equation 7: Matrix representation of Ohm's law for resistor network

A setup similar to that used in ANSYS was used in FastHenry. The free-ends of the three electrical paths were tied to a common port and then electrically grounded. The center pad was then tied to a second port and a frequency of 0.01 Hz was input into the program to generate comparable static (or direct current) simulation results. The results obtained from both programs were identical and their difference from the analytical solution was less than 1%. This result provided confidence in the models, and the other capabilities provided by tools such as inductance and capacitance calculations were believed to be accurate as well.

CHAPTER 6

DESIGN OF THREE-PATH DELTA INTERCONNECT

6.1. INTRODUCTION

Based on the analysis from the Chapter 4, the three-path compliant interconnect design was selected for further study for a number of reasons, as outlined earlier. Its mechanical and electrical characteristics which include the compliance, electrical resistance, and inductance, fall midway between those of the two-path design and the four-path design. The three-path design has the fewest number of paths to give uniform in-plane compliance in all directions. The three paths provide enough compliance, and at the same time ensure that the pad does not rotate in-plane under assembly forces. Also, the three paths provide enough structural stability to withstand normal loads during assembly, ensuring that the center pads stays aligned with the substrate pads.

Although the three-path interconnect has an appropriate compromise between the low mechanical compliance of four-path design and high electrical parasitics of two-path design, the exact dimensions of the three-path design will dictate its mechanical compliance, electrical parasitics, and thermo-mechanical reliability. Accordingly, a parametric study is carried out to determine the effect of key parameters on the mechanical, electrical, and reliability metrics, and thus to determine appropriate dimensions for the proposed three-path interconnect design.

6.2. DELTA INTERCONNECTS

For the sake of brevity and identification, the proposed three-path interconnect design will be called “Delta” interconnect. This is because as illustrated in Figure 6-1, straight lines joining the base supports form a triangular pattern much like the Greek letter Δ, Delta. Also, current flows to and from the center pad through the arcuate structures, just like the delta of a river with its tributaries.

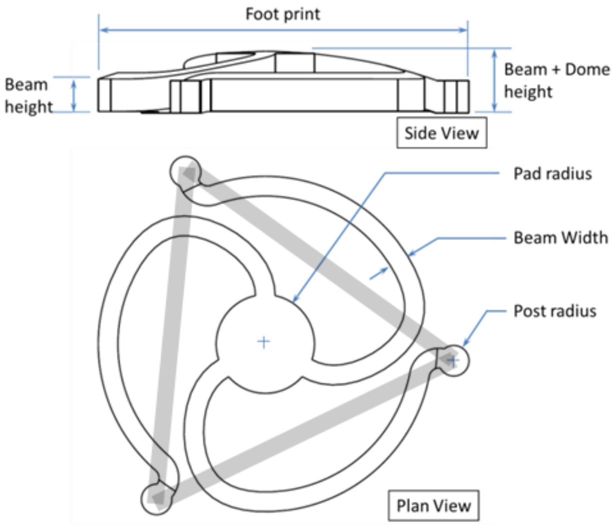


Figure 6-1: Geometric details of Delta Interconnects

To make the Delta interconnect a feasible solution for addressing the low-κ dielectric fracture/delamination issue, its fatigue life had to first be improved. By design, the Delta interconnect accommodates the relative movement of the substrate pad relative to the die pad.

6.3. PARAMETRIC ANALYSIS

In the search for a thermo-mechanically reliable Delta interconnect, a parametric study was performed. The key concerns in this study were to determine how different beam cross-sections influenced the response of the interconnect to mechanical and electrical metrics. The mechanical metrics of interest include compliance (both in-plane and out-of-plane), fatigue life of the interconnects as well as that of the adjoining solder bump. The electrical metrics of interest for this study are the interconnect's resistance and inductance. Capacitance was not included in this study as the proposed interconnect has free-standing arcuate structures without any dielectric material, also in addition, the cross-sectional areas of the arcuate structures are small. Furthermore, the changes in capacitance for the different beam profiles is not enough to warrant a full inquisition of its behavior.

6.3.1. Interconnect Dimensional Parameters

The upper and lower bounds for the interconnect's beam widths and heights used in these simulations were based on the manufacturability of the interconnect at 200 μm pitch. From experience, fabrication of high aspect ratio structures using photolithography could be quite challenging as aspect ratios begin to exceed a value of 3. Aspect ratio, in this context, is the ratio of the thickness of the arcuate structure to the width of the arcuate structure. Yield defects increase with increasing aspect ratios and depending on the type of photoresist being used and the features sizes being patterned, pattern transfer could be adversely affected. Aspect ratios of 1 or less are desirable from a yield and ease of reproducibility point of view. However, based on the mechanics of deformation, an aspect ratio greater than 1.5 is preferred. With an aspect ratio of at least 1.5, the second moment of area for bending deflection in the out-of-plane direction becomes at least 3 times greater than that of the in-plane direction. This is desirable as it ensures that a planar load applied to the center pad will generate deflections only in the in-plane direction. The length of the bending moment arm in the out-of-plane direction is typically greater than the length of the bending moment arm in the in-plane direction, and thus lowering the bending stiffness in the in-plane direction ensures that during thermal excursions that the interconnects will preferentially deform in the in-plane direction. It should be pointed out that the out-of-plane compliance, although desirable to account for the substrate non-planarity, will result in inadequate assembly force and potential vibration-induced damage. On the other hand, the in-plane compliance is desirable to account for the differential lateral displacement between the die and the substrate.

Table 6-1 is a feasibility chart or risk matrix defined by photolithographic capabilities with repeatable results and good overall yield. It lists the arcuate beam geometries used for the simulation study as headers and the resulting aspect ratio of the fabricated beam as entries. Based on the beam's aspect ratios, the fabrication is color coded in terms of ease of manufacturability. The red-colored blocks represent

fabrications with aspect ratios of 4 and greater. In such a case, the yield of the fabrication cannot be guaranteed and hence repeatability of results could be a challenge. Aspect ratios greater than 3 are colored orange. This is within the realm where things can go either way and the fabrication process is sensitive to processing. The three shades of green are the regions within which the fabrication of the interconnects are desired to be. The lower the aspect ratio the higher the probability that all fabricated interconnects will turn out as desired.

The yield of the fabrication not only depends on the aspect ratio, but also on the thickness of the deposited photoresist. To achieve high aspect ratios, a thicker coating of photoresist is usually required. Since the photoresist used in this fabrication is a liquid, thicker coatings are achieved by lowering the spin speed during the coating step. The lower the spin speed the less uniform the thickness of deposited photoresist gets. For spin speeds below 1000 rpm, obtaining a reasonably uniform coating is dependent on a number of factors. A larger than required volume of photoresist is required to ensure that the low centrifugal forces will be strong enough to spread the photoresist across the wafer. The wafer needs to be well centered and the wafer chuck should have no runouts and should be square on the spindle.

Photoresist coating at low spin speeds also result in large edge beads which can interfere with photo exposure of the deposited photoresist to ultraviolet radiation. The edge bead keeps the photomask away from the surface of the photoresist, and in severe cases can distort the imprinted patterns. But a more prominent issue faced with large edge beads is alignment of the photomask to the features on the wafer. Misalignment of the features, if severe, can result in a defective fabrication, therefore ridding the wafer of edge beads for low speed coating is essential. Photoresist manufacturers have various solutions for edge bead removal, and it is recommended to carry out this edge bead removal step to ease fabrication and improve yield.

Table 6-1: Aspect ratio (AR) risk matrix based on photolithography

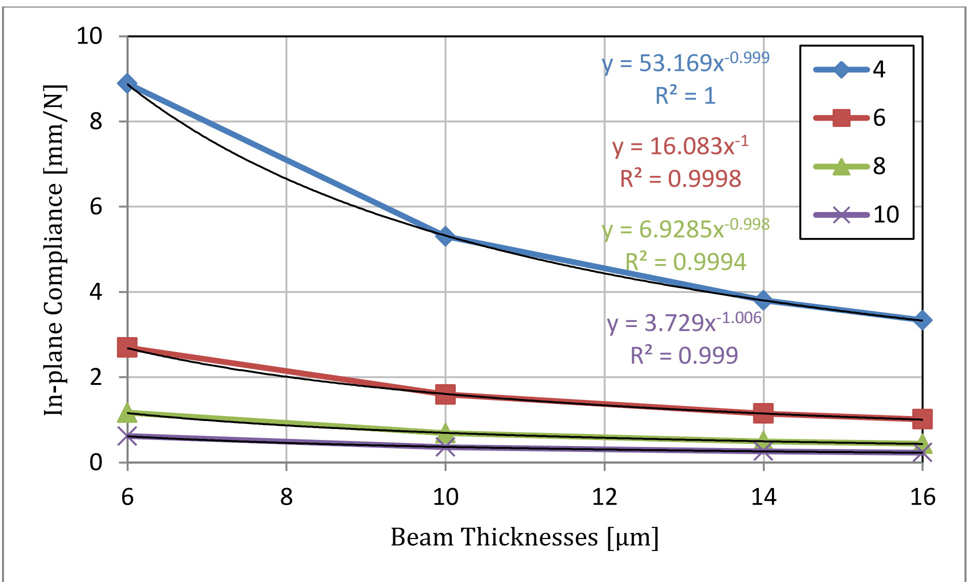
[µm]		Beam Widths [µm]			
		4	**6**	**8**	**10**
Beam Heights	**6**	1.5	1.0	0.75	0.6
	10	2.5	1.7	1.25	1.0
	14	3.5	2.3	1.75	1.4
	16	4.0	2.7	2	1.6

6.3.1.1. Interconnect Dimensions and Mechanical Compliance

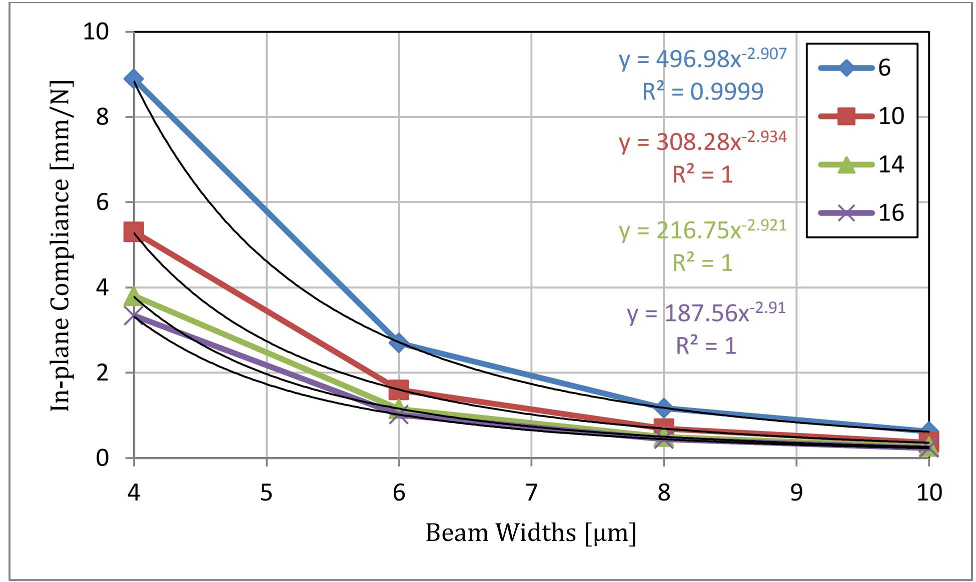
The first set of simulations in this study was performed to understand the effect of arcuate beam cross-section dimensions on the compliance of the interconnects. The setup used for the compliance simulations is described in Section 5.3. Figure 6-2 shows plots of the compliance results. The same information is presented in two ways: the first is a plot of compliance as a function of beam thickness for various beam widths, and the second is a plot of compliance as a function of beam widths for various beam thicknesses. The purpose was to layout the results in such a way that it could be readily identified which parameter had the most influence on in-plane compliance. To also aid in the comparison, trend-lines were fitted to the data and their equations displayed. The plots in Figure 6-2 show that all the curves have a least squares regression fit of 1, suggesting a good fit.

Based on the presented data, it can be seen that for both plots the curves displayed are a family of curves, each plot having the same exponent for its group of curves. The difference in the curves comes from the constant multiplier, which determines the amplitude/magnitude of the curves. The plots in Figure 6-2a representing the in-plane compliance as a function of beam thicknesses has an exponent of negative one (-1), suggesting an inverse decay of compliance with beam thicknesses. The family of curves in Figure 6-2b plots the in-plane compliance as a function of beam widths, and has an exponent of almost negative three (-3). This suggests a more aggressive decay in compliance with increases in beam widths. Or in other words, changes in the beam width

has a more pronounced effect on in-plane compliance than changes in beam thickness. As the flexural rigidity against in-plane bending will scale inversely as the first order of beam thickness and as the third order of beam width, the trends predicted by the simulations are consistent with what is expected.



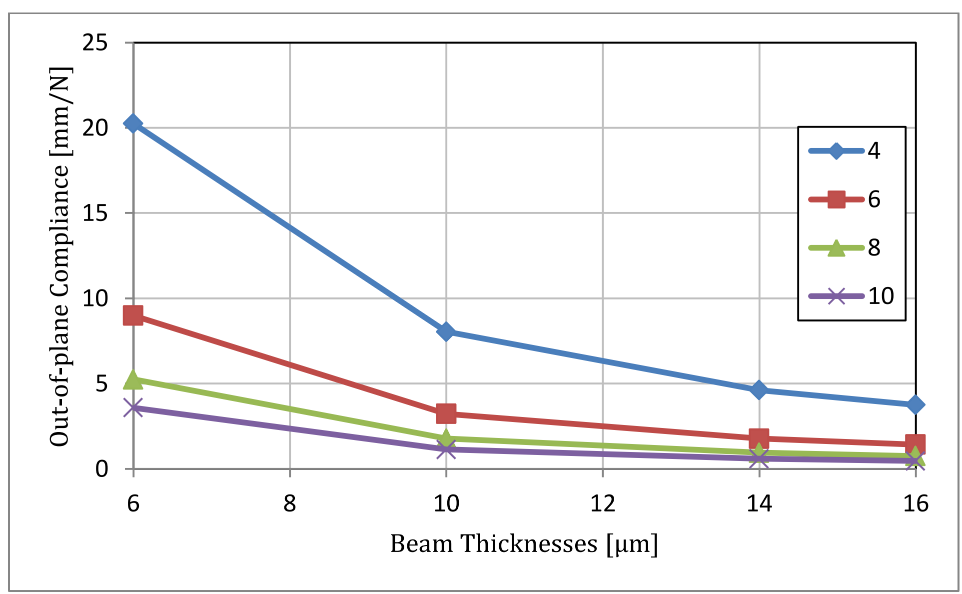
a) In-plane compliance as a function of beam thickness for various beam widths



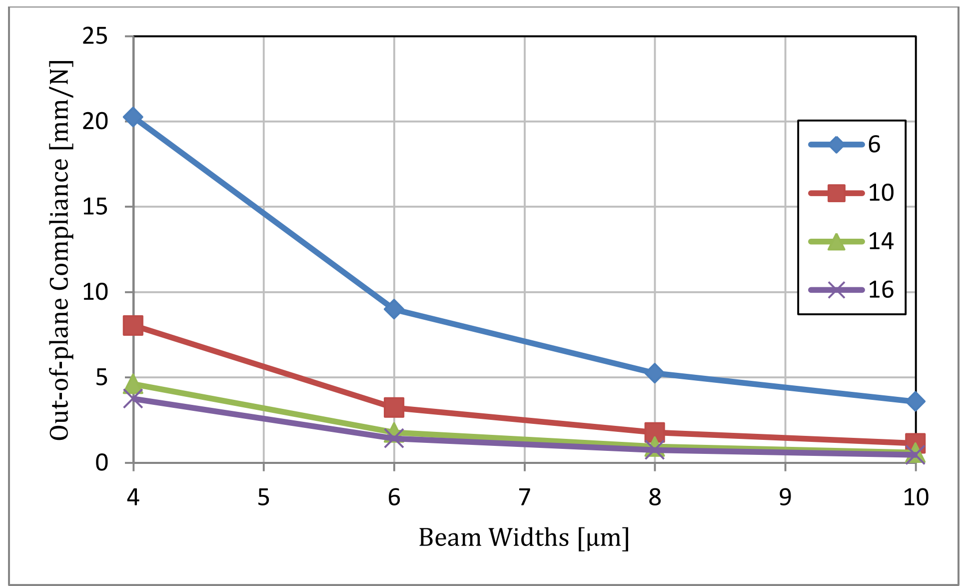
b) In-plane compliance as a function of beam widths for various beam thicknesses

Figure 6-2: Delta interconnects in-plane compliance as a function of its cross-section

A similar exercise was carried out on simulations for the out-of-plane compliance to observe if a trend similar to those encountered with the in-plane compliance plots also exist. For in-plane compliance, the bulk of the deformation of the beam happens in the in-plane direction as result of the displacement load acting along the axis of the beam. This is different for the out-of-plane compliance, as the displacement load acts perpendicular to the axis of the beam. Taking into account the curved shape of the beam, the displacement of the center pad in response to out-of-plane loads is attained through a combination of bending and torsion. This is supported by the observed trend in Figure 6-3, where it can be seen that for increasing beam cross-sections the decay rate of the curves increase. This happens because the beams with larger cross-sections are more resistant to the torsional loads than thinner beams, hence the increase in decay rate. However, like was the case with in-plane compliance, the width seems to have a stronger influence on the out-of-plane compliance than beam thickness.



a) Out-of-plane compliance as a function of beam thickness for various beam widths



b) Out-of-plane compliance as a function of beam widths for various beam thicknesses

Figure 6-3: Out of Plane Compliances

6.3.1.2. Interconnect Dimensions and Electrical Parasitics

Figure 6-4 shows the electrical resistance plots from the study with resistance plotted as a function of beam widths for various beam thicknesses. As seen, the resistance decreases with increasing beam width and increasing beam thickness, and the curves have first-order inverse relationship.

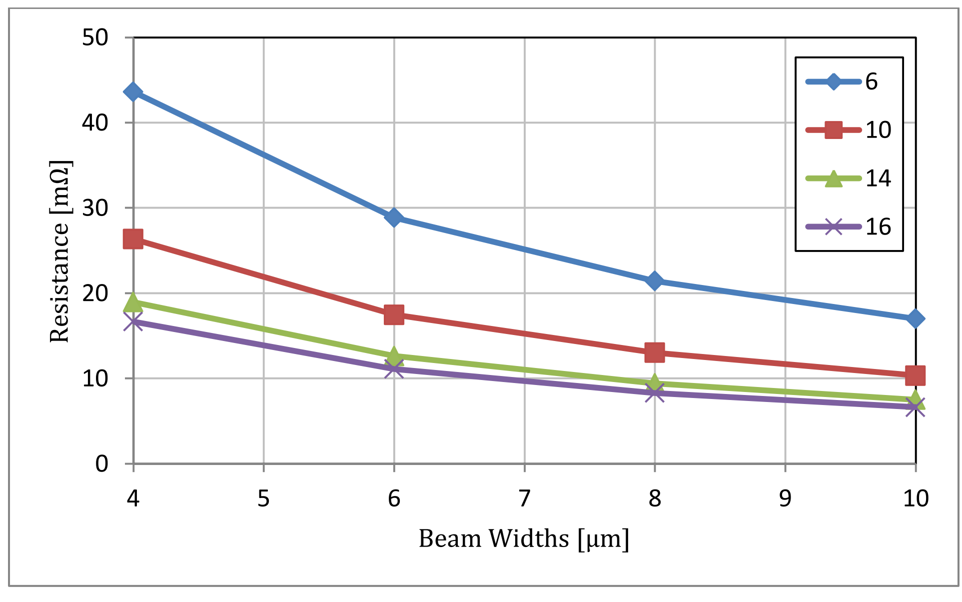


Figure 6-4: Interconnects resistances for various beam cross-sections

Simulations for the changes in inductance of the interconnects for various beam dimensions was also conducted. The inductive response of the interconnects was not one of the criteria for the selection of a suitable interconnect geometry. However, the simulations help complete the characterization of the response of the interconnects to stimuli. From Figure 6-6 it can be observed that the changes in inductance appear to be linear for each of the beam thicknesses and the rate of change of inductance with respect to the width of the beam is mild. For instance, there is only a 5 pH drop in inductance between a 4 µm wide beam and a 10 µm wide beam. Figure 6-5 illustrates the proximity effect by comparing the clearance between neighboring interconnects for a 4 µm wide beam and a 10 µm wide beam as indicated by the red arrows. The close proximity of the beams seems to have an attenuating effect on the magnetic fields generated around the interconnects. In all, the changes in inductance for various interconnect dimensions are small, with minimal design consequence. It should be pointed out that in all of these simulations, the shape and length of the arcuate structures remained the same, and the only parameters that changed were the width and thickness of the arcuate structure. Thus, the change in inductance with the dimensional change was minimal, as would be expected.

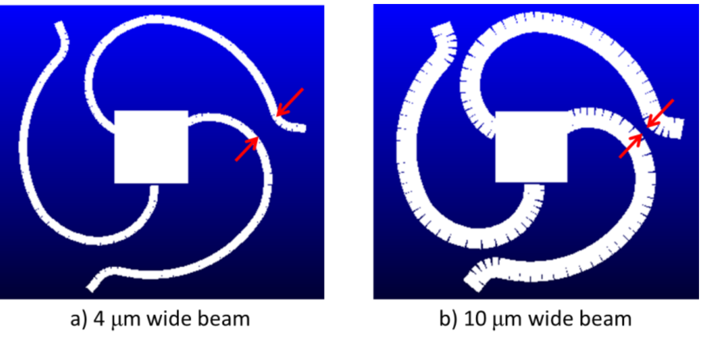


Figure 6-5: FastHenry models for inductance simulations

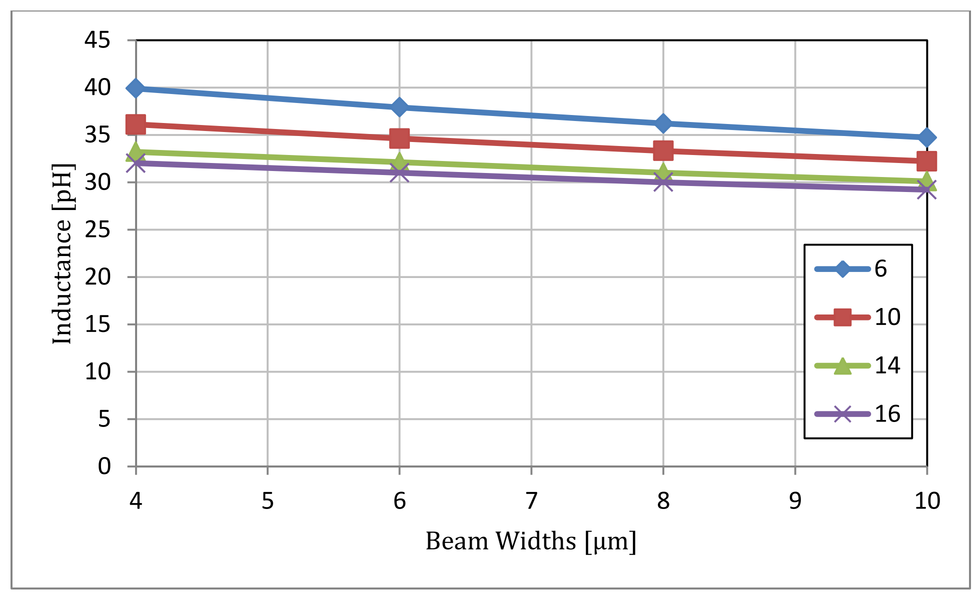


Figure 6-6: Inductive response of interconnects for various beam cross-sections

6.3.1.3. Interconnect Dimensions and Thermo-Mechanical Fatigue Life of Compliant Structure

Fatigue life simulations for various interconnect cross-sections also show a decaying trend with respect to increases in the beam's cross-section. The change in fatigue life with respect to the beam's width shows a more pronounced change for beam widths less than 6 µm as shown in Figure 6-8. However there is no observable trend with changes in beam thickness. The plot shows the results for the various simulated beam thicknesses clustering together for various beam widths. As a design tool, this plot did not provide meaningful information to guide the selection of appropriate dimensions for the interconnect cross-section. Examining the failure locations of the interconnects for each of the data points, it was observed that the failure location oscillated between two prominent locations. The first site of failure is near the center pad while the second failure site is close to the anchor/base of the interconnect. The algorithm used in the determination of fatigue life of the interconnects scans the entire elements of each interconnect for the most strained element, which is likely the initiation point for a crack. Depending on the cross-section of the interconnect and its deformation pattern, the most

strained element appears at either of the failure sites indicated in Figure 6-7. The volume weighted average of the accumulated plastic strain of this element and its immediate surrounding elements is used in a Coffin-Manson-type predictive equation to determine the fatigue life of the compliant interconnect.

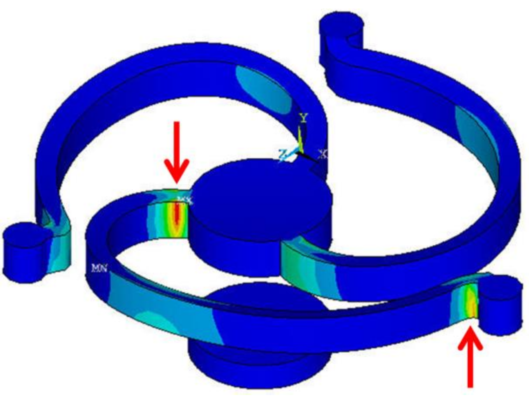


Figure 6-7: Two observed interconnect failure locations based on finite element predictions

To obtain a more consistent trend in the fatigue life results, a common failure location was selected for all models. Figure 6-9 shows the plots of fatigue life against beam width for a failure location near the base of the interconnects. Selecting a common failure location for all the interconnects works better for the sake of comparing changes in the geometric parameters of the interconnect. A distinct trend can now be observed in the data, which shows a decay of fatigue life with increasing beam width and thus decreasing compliance. Considering that the largest interconnect modeled has a width of 10 μm and a thickness of 16 μm; these structures are extremely compliant when compared with the 500 μm thick die and substrate. Hence during thermal excursions, the net displacements experienced by the center pads of the different interconnect geometries is very nearly the same. In such a case, it can be seen why a wider beam will have a much shorter fatigue life. Since the beams are subject to the same displacement load, the wider beams reach critical stresses and plastic strains sooner. In other words, a narrower beam is more flexible and hence better equipped to accommodate large tip (center pad) deflections than a wider beam.

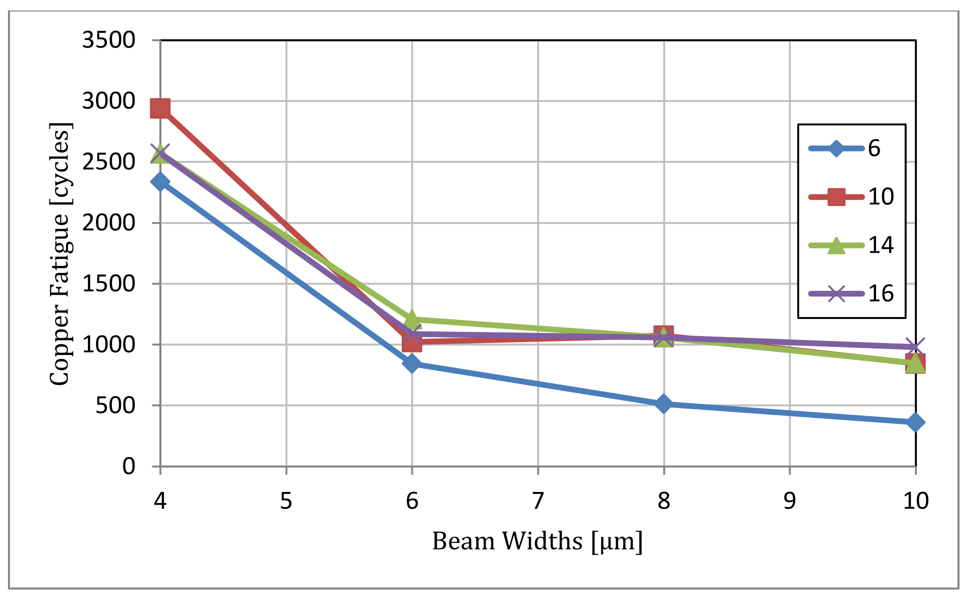


Figure 6-8: Interconnect fatigue life based on highest strained element location

The influence of beam thickness of the fatigue life data is somewhat muted. This is possibly due to three competing reasons: 1) thermo-mechanical deformation is primarily lateral, and thus, the thickness (out-of-plane dimension) has a much lower effect than the width in resisting bending deformation, as discussed earlier. 2) The fatigue life computations are based on volume-averaged strain, and thicker structures have a lower volume-averaged value. 3) As in wider structures, thicker structures have higher stiffness, and in general and in general are expected to have higher stresses and plastic strain. Thus, the three competing mechanisms make the change in fatigue life with respect to thickness non-monotonic.

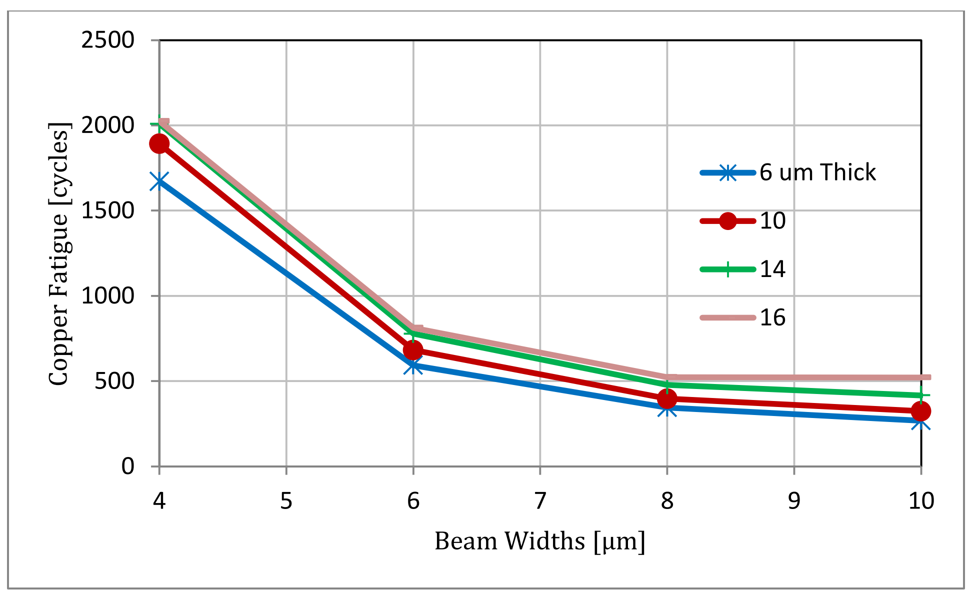


Figure 6-9: Interconnect fatigue life based on a common failure location

6.3.1.4. <u>Interconnect Dimensions and Thermo-Mechanical Fatigue Life of Solder Joints</u>

The fatigue life of the solder joints connecting the interconnects to the substrate was also simulated. These simulations were to ensure that failure of the solder joints will not precede the failure of copper interconnects. From the reliability numbers determined for the solder joints, it is clear that failure of the solder joints will not precede the failure of copper structures in the compliant interconnect. For this reason, other failure modes prominent for flip-chip solder joints, such as the formation of intermetallic compounds at the interfaces of copper and solder and the resulting embrittlement of the joints will not be considered in this work. With the solder bumps having a cross-sectional area of about 1200 μm^2 and a compliance of about 0.004 mm/N compared with the interconnects total combined cross-sectional area of 480 μm^2 and compliance of about 1 mm/N for the largest interconnect simulated, it can be seen that failure will not occur in the solder joints. As a consequence of the interconnect's compliance, the reliability of the interconnection technology is relatively insensitive to temperature ramp rates, and can pass quickly through extreme temperature cycles with no impact to the fatigue life. This

is because the weakest link in the interconnect is the copper arcuate structure, which does not have time-dependent creep deformation in the temperature ranges under consideration.

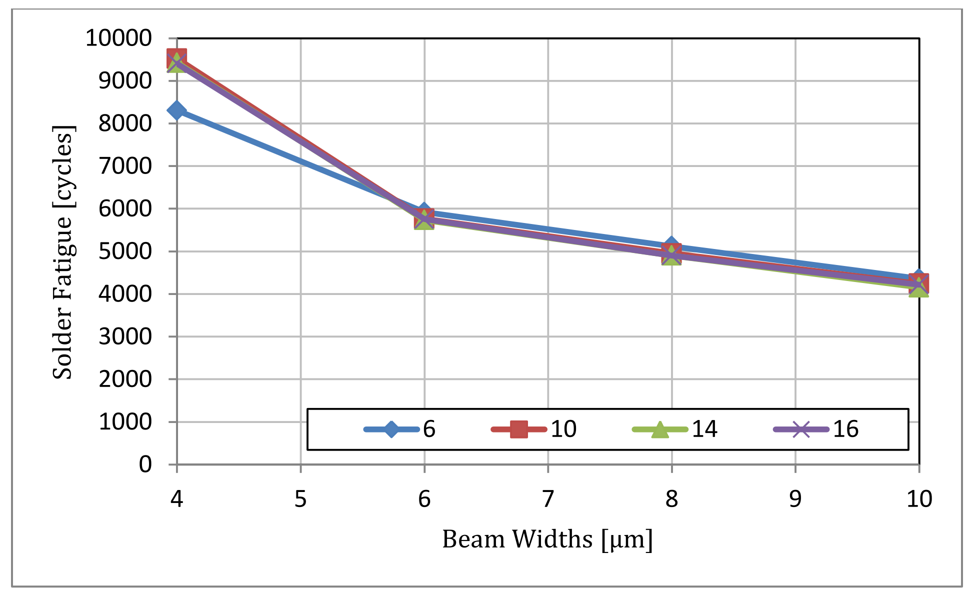


Figure 6-10: Solder fatigue life based on highest strained element location

To support this claim, two identical models were created and subjected to the same temperature extremes. The first model was cooled from 220 ^{o}C to 25 ^{o}C over a period of 1 min. The second model was slowly cooled between the same temperatures over a period of 60 min. As shown in Figure 6-11, the plastic strain profiles in both solder joints are similar. However, the largest amplitude strain is observed on the solder that was rapidly cooled. This localized maximum strain is believed to be as a result of undersized sized elements in the solder. The slow cooled assembly on the other hand, shows a more uniform and higher overall strain in the solder bump. The slow cooling of the assembly allows creep deformation (which is a time dependent phenomenon) to take place. However, both of the strain values in the solder joints are low, even though the percentage increase in plastic strain from cooling the model slowly is about 11%. In both models, the fatigue life of the interconnects came out to be about the same and the failure

location was also in the same location in the arcuate beams of the interconnects. This means that this technology can be used for severe applications where temperatures can swing wildly like in space vehicles subjected to the intense radiant heat from the sun at one instance and then to the frigid cold of outer space at another.

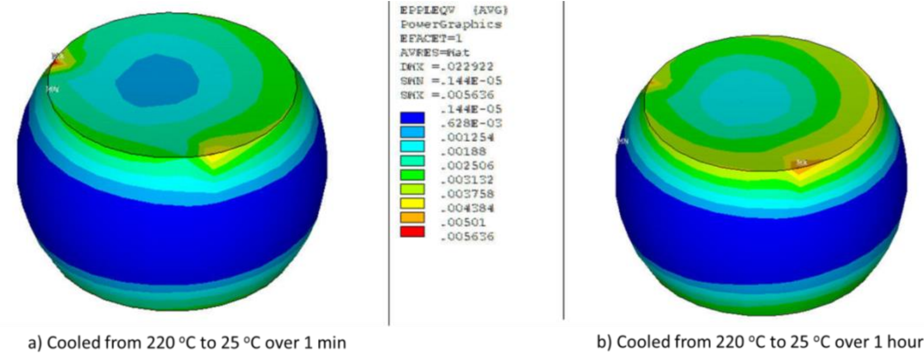


Figure 6-11: Plastic strain in solder bump comparison between a rapidly cooled assembly and a slowly cooled one

In addition to the cool down comparison, another pair of models were created to observe the impact of thermal shock on the fatigue life of the interconnects and solder. The models were cycled between temperatures of 0 to 100 ^{o}C. The ramp rates for the cool down and heat up steps was set to 100 ^{o}C/min for the thermal shock model while the thermally cycled model's ramp rates were set to 15 ^{o}C/min as per JEDEC specifications. Table 6-2 lists the results from the study. From the results, there is no influence of temperature ramp rate on the fatigue life of the Delta interconnects. The solder bump on the other hand shows a slight increase in fatigue life for the thermally shocked model. The gain can be attributed to the lower overall gain in creep strain as the cycle rate exceeds the creep deformation rate. However, the change in solder fatigue life is only about 4%.

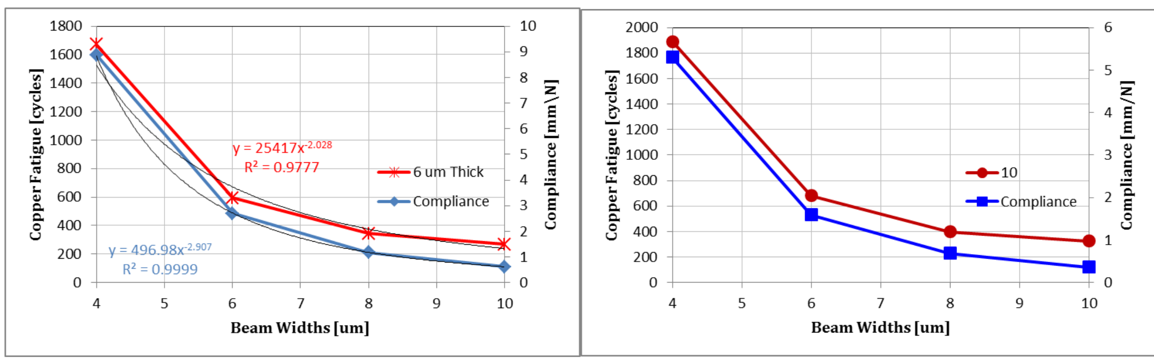
Table 6-2: Thermal cycling vs Thermal shock of Delta interconnects

	Thermal Shock	**Thermal Cycle**
Ramprate [^{o}C /min]	100	15
Interconnect life [Cyc]	871	872
Solder life [Cyc]	6140	5990

6.3.2. Compliance vs Fatigue life

There is a common belief that an increase in compliance equates to an improvement in fatigue life. This notion may have stemmed from the idea that compliant interconnects are the solution for copper/low-κ technologies. By way of analogy, if this statement is true, then a compliant short spring with a relatively short free-length should outperform a longer stiffer spring subjected to identical displacement loads. Clearly this argument does not hold for displacement loads greater than the free-length of the short spring, and it also does not hold true for displacement loads within the limits of elasticity of the short spring. This is because displacement loads within the limits of elasticity of the short spring also fall within the limits of elasticity of the stiffer spring. Hence, the outcomes will be similar.

To test this belief, results from the design study were compiled for fatigue life versus the compliance of each of the variants modeled. The plots in Figure 6-12 show a strong correlation between fatigue life and compliance for each of the beam thickness modeled. In this case, however, the interconnects being analyzed are identical in terms of their free-lengths. The only differences come from the cross-sectional widths. As described earlier, the interconnects with wider beams will have a shorter fatigue life as they will attain higher surface strains. With these compliant interconnects, the deformation load incident on the interconnects is approximately the same for both the narrow and wide beams. This is expected because the physical size of the interconnects is much smaller than the die/substrate cross-sections which they are trying to resist.



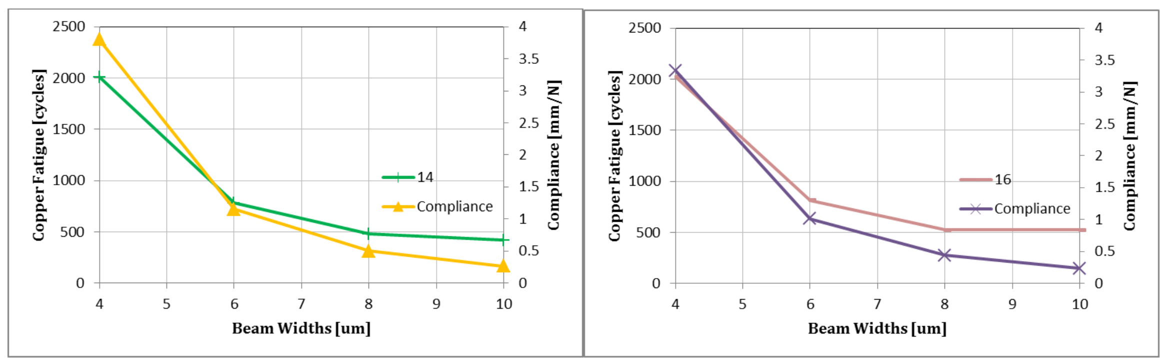


Figure 6-12: Compliance vs Fatigue life as a function of beam width for various beam thicknesses

When all the results from the 16 simulated cases are plotted as a single graph shown in Figure 6-13, it is seen that lower compliance interconnects generally have a lower fatigue life. In the same manner, higher compliance interconnects are shown to have higher fatigue lives but there seems to be a point beyond which additional increases in compliance does not much of an impact on the fatigue life of the interconnect.

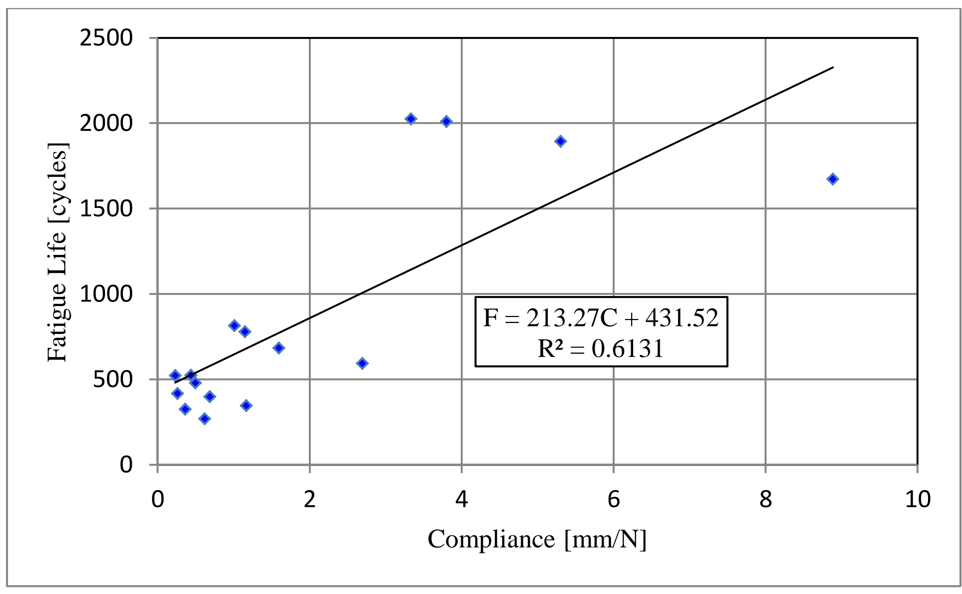


Figure 6-13: Fatigue life as a function of Compliance for explored geometries of Delta Interconnects

6.3.3. Geometry selection

Based on the parametric study, the following criteria were set in the design of the compliant interconnect:

- The interconnect has to be manufacturable
- The interconnect should be compliant enough so that the stresses induced in the die are small.
- The interconnect must be able to attain the minimum fatigue life requirements
- The interconnect should have reasonable electrical parasitics (resistance)

Based on the first criterion, the aspect ratios of the arcuate beams of the interconnect had to be selected from the green colored cells in Table 6-1. A target aspect ratio of 2 is desired, since firstly, it falls within the capabilities of most photoresists and secondly, an aspect ratio greater than 1 reduces the likelihood of torsional deformation of the beams. The presence of torsional loads creates complex stress states within the beam that can adversely impact its fatigue life.

In terms of meeting the minimum fatigue life requirements, the plots from Figure 6-8 show that interconnects with beamwidths of 6 μm and less are capable of achieving 1000 fatigue life cycles and more. However, while it is desirable to select a beamwidth which gives the most fatigue life cycles, this end goal conflicts with the last design criterion associated with reasonable electrical parasitics. From Figure 6-4, there is a 50% increase in resistance by selecting a 4 μm wide beam as opposed to a 6 μm wide beam. Since a target life of 1000 cycles is desired, a 6 μm wide beam was selected to minimize the electrical resistance of the interconnect.

Since an aspect ratio of 2 is desired, the final dimensions of the interconnect selected for fabrication was a 6 μm wide beam with a target thickness of 12 μm. However, since the thickness of the interconnect is only bounded by the capability of the photoresist, it is possible to shoot for higher interconnect thickness as this can improve fatigue life as shown in Figure 6-9 and further lower electrical resistance as shown in

Figure 6-4. However, increasing the beam's thickness increases its surface area which could potentially increase the interconnect's capacitance.

6.3.3.1. Directional Dependence of Fatigue Life

In Chapter 4, it was shown that for stable rotationally symmetric interconnect designs, the in-plane compliance is independent of the orientation of the applied load. The applied loads in those simulations were small loads to prevent plastic deformation of the interconnect which would artificially increase the interconnect's compliance. However, for fatigue life tests particularly in the low cycle regime, there is a greater amount of plastic deformation within the compliant arms of the interconnect. To understand the impact of plasticity on the fatigue life of the interconnect with respect to orientation, a GPD model as described in the previous chapter was created. Only one interconnect, representing a peripheral row of interconnects was simulated to reduce computational time. The interconnect's orientation was rotated 10 degrees for each run for a total of 12 runs. The twelve runs span an angle of 120°, which is sufficient to fully describe the behavior of a tripod structure.

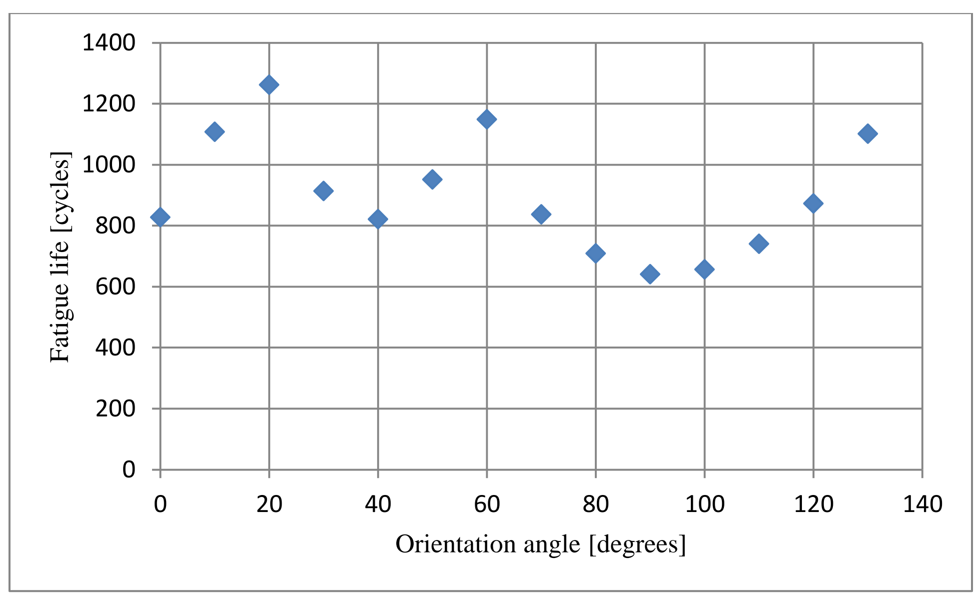


Figure 6-14: Fatigue life of interconnect as a function of orientation

The result of the simulation is presented in Figure 6-14, where the data suggests some dependence of fatigue life on orientation. Figure 6-15 shows the orientation of the interconnect at 10 degrees. The orientation angle is determined by the angle the end of the arcuate beam makes with the radial line drawn from the neutral point of the die through the center of the interconnect. From the plot in Figure 6-14, the best orientation of the interconnect spans at least the first 60 degrees of orientation angles. Statistically, this implies that a randomly oriented interconnect has a 60% chance of having a fatigue life greater than 800 cycles. This range gives some leeway in the placement of the interconnects to achieve thermo-mechanical reliability targets. For the mask design, however, the orientation dependent life of the interconnect was taken into account in the mask design process to ensure that the interconnects were favorably oriented to meet design expectations.

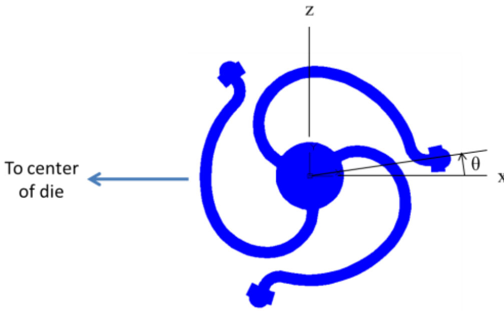


Figure 6-15: Default orientation of Interconnect for orientation dependent fatigue life study

6.4. CHARACTERISTICS OF SELECTED DESIGN

6.4.1. Electrical

6.4.1.1. Frequency Dependent Parasitics

The final selected interconnect geometry has a 6 µm wide beam that is 12 µm thick to maintain an aspect ratio of 2. For fatigue life considerations, this interconnect will be oriented at an angle of 10 degrees based on a line drawn through the neutral point

of the die. Based on this geometry more comprehensive tests detailing the interconnects full response to electrical stimuli is performed. The frequency dependent electrical parasitics of the interconnect is plotted in Figure 6-16.

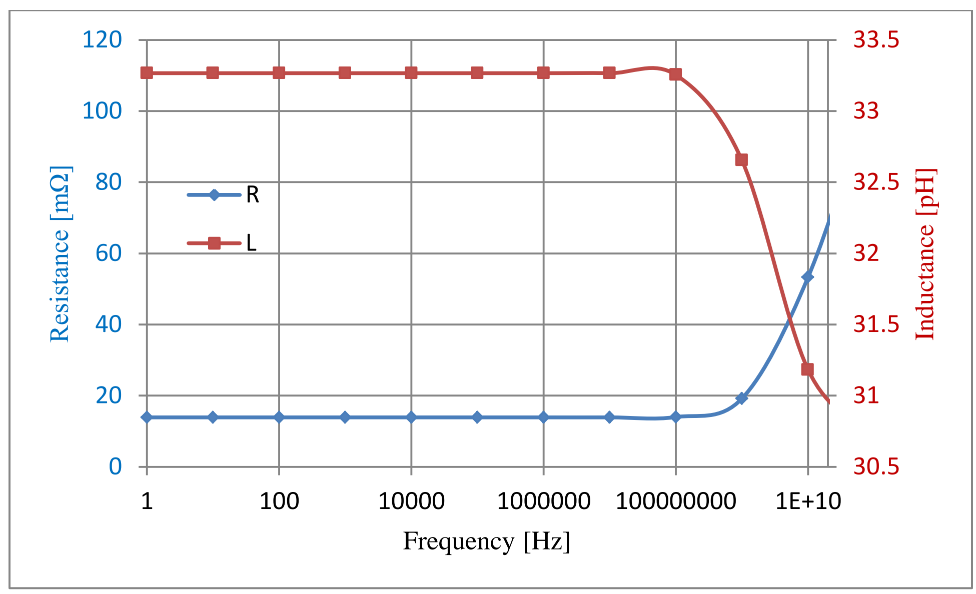


Figure 6-16: Full RL response of Interconnect up 20 GHz

The plots show that the RL parasitics of the Delta interconnect remains steady up to a frequency of 1 GHz beyond which skin effects begin to degrade the electrical resistance. At 20 GHz, the electrical resistance degrades by 500% of its original value while some improvement in inductance is observed. Assuming the capacitance of the interconnect remains steady through these frequencies, a degradation of the time constant of the interconnects will be observed for frequencies greater than 1 GHz. This frequency is considered to be the cutoff frequency, as the electrical parasitics of the interconnects start to degrade beyond this point.

6.4.1.2. Redundancy

Delta interconnects, by design, are multi-path structures which imply that their construction incorporates redundant electrical paths. In the case of a failure of one of the paths during service, the affected interconnect does not fail abruptly, but undergoes a transition to a lower operating state, where its electrical parasitics are slightly increased.

This is best exemplified with simulations of failed electrical paths. Models simulating failures in one or two electrical paths were created. These simulations describe how the resistance changes as fatigue failures begin to occur across the different electrical paths. The change in electrical parasitics of the interconnect with path failures is illustrated in Figure 6-17. With no failures, the resistance and inductance values remain at the levels reported earlier. When one path fractures, the interconnect will still function due to the two remaining electrical paths, and the interconnect resistance and inductance will increase by about 50% compared to the initial resistance and inductance values. When two paths fracture, and that is, with only one functional path remaining, the resistance and inductance values are about three times the original values.

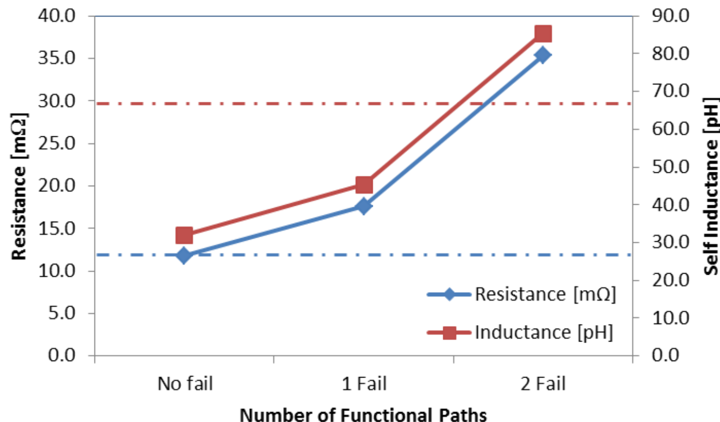


Figure 6-17: Interconnect resistance for: No failures, 1 path failure and failure of 2 paths

The reference horizontal lines shown in Figure 6-17 represent the resistance (lower line) and inductance (upper line) of a single-path interconnect design with the same total cross-sectional area as the multipath design. From Figure 6-17, it is seen that both single-path and multipath designs have the same electrical resistance but the multipath design has inductance values less than half that of the single path design. This shows that a multipath design has superior electrical parasitics when compared with a single path design. Also, the multipath design offers higher mechanical compliance as

well as redundant electrical paths. It is noteworthy to mention that the simulated single-path and multipath designs had the same electrical path lengths.

When one of the paths fails, the mechanical compliance of the three-path interconnect will increase, and the interconnect will still be functional. Preliminary studies indicate that the remaining two paths will remain functional through several additional hundred cycles.

Hand Calculation	FastHenry	Ansoft Q3D
14.1 mΩ	14 mΩ	14 mΩ
-	58.8 pH	58.8 pH
R2, R1, R1, R2, R1, R2		

To completely characterize electrically the parasitics of the interconnects in an assembly configuration where the on-chip traces and substrate traces are present with solder bumps connecting the interconnects to substrate pads, a 2 x 2 layout of interconnects with a pitch of 200 μm was created sitting atop a 500 μm thick dielectric material with an 18 μm thick ground plane attached beneath (depicted in Figure 6-18). Ports were then assigned to each of the interconnect assemblies, and the simulation run for direct current (DC) response and alternating current (AC) response at 1 GHz. The ground plane beneath the dielectric material is referenced as Copper_clad in the models, while the interconnect assemblies are referenced as Copper_pads. The dielectric medium surrounding the interconnects (Copper_pads) is air since this technology does not utilize

underfills. The absence of the underfill material helps ensure that the capacitance of these structures is minimal since air has the lower dielectric constant of available materials.

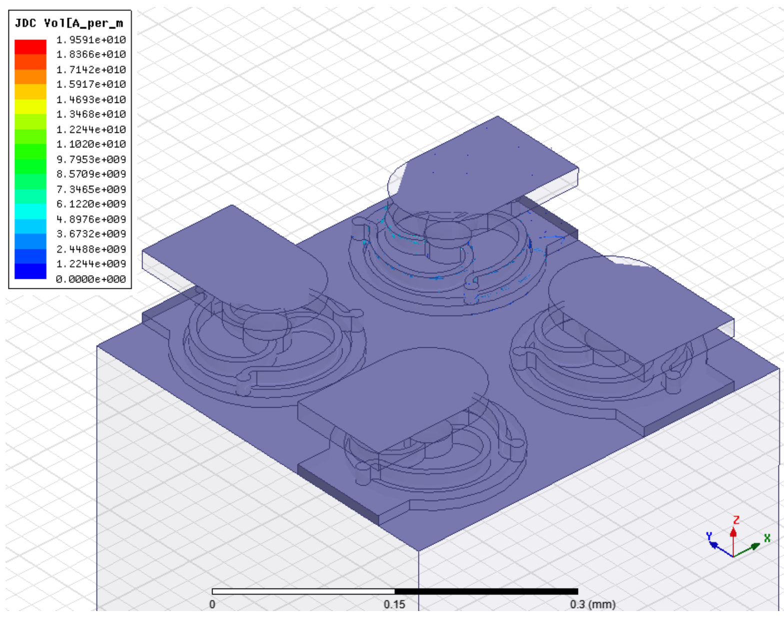


Figure 6-18: Ansoft Q3D model for RLC characterization of the interconnects

From the DC results in Table 6-3, the resistance of the interconnect assembly is increased to 16.4 mΩ. The 2.4 mΩ increase comes from the bump included in the model. A 40 µm diameter solder ball made of SnAg with a resistivity of 7.78e-8 Ω/m and a length of 40 µm will yield this value. This suggests that the values check out. The table also lists the DC inductance values for self-inductance of the interconnects as well as their mutual inductance. The self inductance of the assembly works out to 71.7 pH, while the mutual inductance between neighboring interconnects works out to about 1.75 pH for adjacent interconnects and 1.17 pH for the interconnects at diagonals. The low mutual inductance values suggest good decoupling of Delta interconnects. This implies that the tendency for cross-talk between interconnects is greatly reduced, and the fidelity of the transmitted signals will be very high. The inductance values are even lower for AC signals reducing in magnitude by about 35%. The electrical resistance, however, as a result of skin effect, increases by about 160%.

Table 6-3: DC response of interconnects for resistance and inductance

	COPPER_PAD_1:Source4	COPPER_PAD_2:Source1	COPPER_PAD_3:Source2	COPPER_PAD:Source3
Freq: 1 (GHz)				
COPPER_PAD_1:Source4	0.016395, 0.071681	0, 0.0017642	0, 0.0011735	0, 0.0017517
COPPER_PAD_2:Source1	0, 0.0017642	0.016377, 0.071613	0, 0.0017597	0, 0.0011699
COPPER_PAD_3:Source2	0, 0.0011735	0, 0.0017597	0.016383, 0.071564	0, 0.001757
COPPER_PAD:Source3	0, 0.0017517	0, 0.0011699	0, 0.001757	0.016397, 0.07164

Table 6-4: AC response of interconnects @ 1 GHz for resistance and inductance

	COPPER_PAD_1:Source4	COPPER_PAD_2:Source1	COPPER_PAD_3:Source2	COPPER_PAD:Source3
Freq: 1 (GHz)				
COPPER_PAD_1:Source4	0.042363, 0.046808	0.00069734, 0.00074207	0.00044684, 0.00039413	0.00070223, 0.00074337
COPPER_PAD_2:Source1	0.00069734, 0.00074207	0.042438, 0.046788	0.00069377, 0.00073987	0.00045085, 0.00039121
COPPER_PAD_3:Source2	0.00044684, 0.00039413	0.00069377, 0.00073987	0.042388, 0.046793	0.00069688, 0.00075248
COPPER_PAD:Source3	0.00070223, 0.00074337	0.00045085, 0.00039121	0.00069688, 0.00075248	0.04238, 0.046775

In a separate report, the capacitance of each interconnect assembly and their capacitance relative to neighboring conductors was also recorded. The self-capacitance of the interconnects is about 36 fF. Its capacitance relative to neighboring interconnects is about 11 fF for adjacent interconnects and about 5 fF for diagonal members. These results show the Delta interconnects to have low electrical parasitics, which positions this technology for use in high performance systems.

[*f*F]	Cu_Clad	Cu_Pad	Cu_Pad_1	Cu_Pad_2	Cu_Pad_3
Cu_Clad	27.45835	-3.46907	-3.48322	-3.47275	-3.4697
Cu_Pad	-3.46907	36.11808	-10.91356	-5.101928	-10.9106
Cu_Pad_1	-3.483215	-10.91356	36.25541	-10.89157	-5.11608
Cu_Pad_2	-3.47275	-5.101928	-10.89157	36.17228	-10.89938
Cu_Pad_3	-3.469695	-10.9106	-5.11608	-10.89938	36.12798

6.4.2. Mechanical

In addition to compliance tests for both in-plane and out-of-plane compliance of the interconnects, a fully populated strip model with about 50 interconnects spaced at 200 µm pitch was created. Using the same test conditions as previous simulations, JEDEC JESD22-A104D-J, which calls for temperature cycle limits between 0 to 100 ^{o}C, the

response of the assembly was simulated. The overall principal stress within the die at room temperature is shown in Figure 6-19. This stress can be seen to vary between -1.11 MPa and 3.33 MPa. The extremely low die stress is a result of the high compliance of the interconnect. The high compliance of the interconnect decouples the die from the substrate, and therefore, reduces the die stress. This is evidenced by the low die warpage depicted by the out-of-plane (y-direction) displacement plot shown in Figure 6-20. The overall warpage of the die was calculated to be approximately 5.5 μm over a distance of 10 mm (half the die length). This warpage value falls within the surface variations of laminates/test boards, and hence, could be considered negligible.

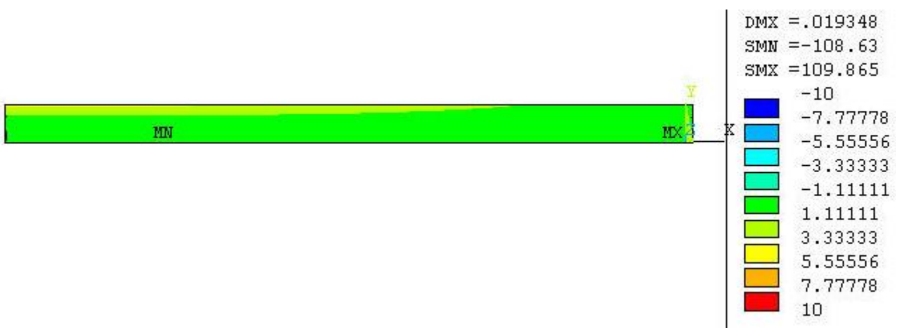


Figure 6-19: First principal stress (MPa) in die at room temperature

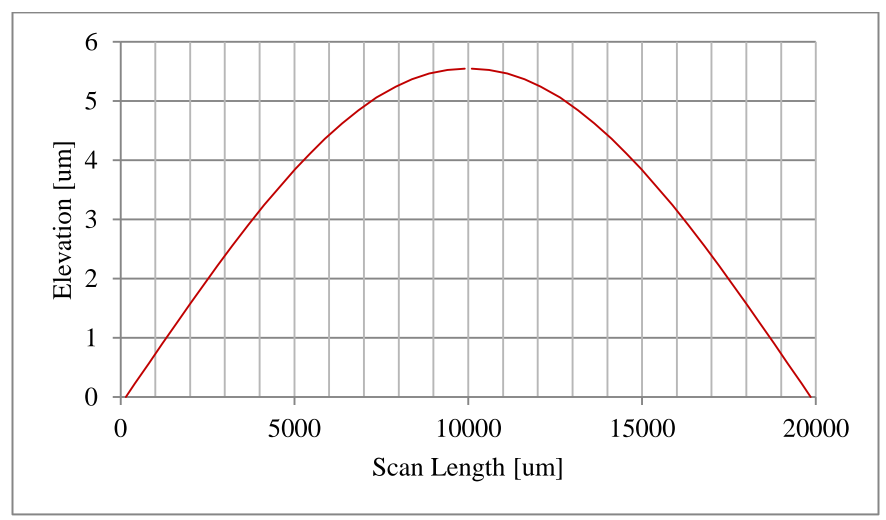


Figure 6-20: Die curvature at room temperature

In summary, through several models and simulations, an interconnect geometry capable of achieving design targets was selected. This interconnect has dimension of 6 μm and 12 μm for its beamwidth and beam thicknesses respectively. Thermo-mechanical simulations of fatigue life puts the service life of these interconnects above 1000 fatigue life cycles. The general responses of the interconnect based on direct inquisition of responses such as compliance and electrical parasitics have been listed in Table 6-5. The responses of the interconnect in package assemblies are also included in the table. It will be noticed that these interconnects reasonably decouple the die from the substrate during thermal excursions. This is evidenced by the low die stresses and die warpage in the assembly. In addition to low die stresses, since the compliance of the interconnects is dependent on the copper based arcuate beams, this interconnect solution is insensitive to environments with rapidly changing temperatures. This property stems from the material of construction, copper, which is a thermally stable material between the operating temperatures of most electronic devices. Finally, the multi-path nature of the delta interconnect prevents catastrophic failure of devices employing this technology by allowing for a transition to a lower operating state which could be configured in such a way to notify the operator of the failure in the interconnect.

Table 6-5: Properties of Delta Interconnects

Properties	Values
In-plane Compliance [mm/N]	1.33
Out-of-plane Compliance [mm/N]	2.31
Resistance (DC) [mΩ]	13.9
Inductance (DC) [pH]	33.3
Capacitance [fF]	3.48
Fatigue Life Cu [Cycles]	~1200
Fatigue Life solder [Cycles]	>5000
Die Warpage [μm]	5.5
Die Stress [MPa]	~3

CHAPTER 7

FABRICATION OF COMPLIANT INTERCONNECTS

The key aspect in the development of any technology is in the ability to bring such a technology to realization. Only through fabrication of the interconnects can it be ascertained if the design is truly capable of achieving simulated results. Some considerations taken into account in the development of fabrication procedures to realize the proposed interconnect design include cost, repeatability, yield and performance.

As described earlier in section 3.1. , cost is a big factor that determines if a design would be successful or not in gaining acceptance. A manufacturing technique to realize a low cost implementation is through batch fabrication. In batch fabrication, the creation of the interconnects on the dies is done at the wafer level prior to die singulation. Depending on die size and wafer size, the number of interconnects that are simultaneously fabricated could number in the thousands which help lower fabrication costs.

Process repeatability and product yield go hand-in-hand. A repeatable process would likely result in high yield. With this in mind, and with the knowledge that fabrication of these devices is carried out at the micron scale, established fabrication techniques, such as those employed in CMOS processing are adopted for this work. This ensures that the fabrication solution is compatible with current industry capabilities without the need to invest in additional infrastructure.

Performance is perhaps the ultimate test of the interconnect's ability to meet design targets and this comes after fabrication is completed. Dies employing this interconnect technology will be assembled and thermally cycled to determine its thermo-mechanical reliability. Electrical characterization tests will also be conducted to give a clear understanding of the physical capabilities of the interconnect design.

This chapter goes over the fabrication details employed in the realization of the compliant interconnect design. Specifically, an overview of the fabrication procedure is

first given. This is followed by the selection of photoresist for fabrication of the interconnect. An in-depth description of the fabrication follows after this. Lastly, the resulting compliant interconnects from the fabrication process are presented and discussed.

7.1. MICRO-FABRICATION OVERVIEW

Lithographie, Galvanoformung, Abformung (LIGA), which stands for Lithography, Electroplating and Molding, is a German-developed micro-fabrication technique using x-rays to produce high aspect ratio structures in photosensitive polymers [68]. Owing to the inherent radiation danger associated with x-rays and the costs of such an operation, micro-fabrication has since moved to what is now known as a LIGA-like process which uses the same principles, but in this process, the x-ray source is replaced with ultra-violet radiation. LIGA-like processing is by far the dominant micro-fabrication methodology used in the micro-electronics industry for the fabrication of micro-devices.

During compliant interconnect fabrication, photoresist is applied to the wafer that is being processed. The wafer is then loaded into a mask aligner, a tool for aligning the photomask to features on the sample and for exposure after alignment is complete. During exposure, the glass mask casts a shadow of the imprinted pattern on photosensitive polymers in the photoresist deposited on the samples being processed. Depending on the feature sizes intended, a suitable light source with wavelengths capable of achieving the desired pattern dimensions is selected.

After the patterns have been transferred to the samples and developed, the developed features then serve as micro-molds or etch masks through which additive buildup or subtractive etch processes are respectively used to create the intended structures. This completes the concept on LIGA-like fabrication which is the basis for the fabrication of the Delta interconnects. Extensive details on micro-fabrication can be found in number of sources [69].

7.2. PHOTORESIST SELECTION

Photoresists which are composed of polymers with light-sensitive molecules attached to its chains are enabling technology for micro-fabrication. Depending on the type of photoresist, positive or negative, a positive or negative image of the mask respectively is transferred to the sample. For example, for a positive photoresist, an opening on the mask becomes a trench in the sample, and the converse is true for negative resists.

Over the course of this research, three different size scales of interconnects, 100 μm, 200 μm and 400 μm pitch, were fabricated. But, for the sake of brevity, this discussion will be limited to the fabrication of the 200 μm pitch interconnects. Fabrications at both the lower and higher pitch sizes employ the same fabrication procedures with the exception of use of other photoresist types to generate these structures.

The photoresist used in the 200 μm pitch fabrication was SPR220-7™ manufactured by Megaposit®. SPR220 is an *i*-line positive tone general-purpose photoresist with broadband capabilities. The benefits of this photoresist are its low exposure dose requirements and excellent adhesion to copper and silicon. It also has excellent plating characteristics, both in copper and solder plating baths. Swelling issues during development were not observed with this resist, and samples can be overdeveloped without ruining the patterning process. Based on the image tone of SPR220, it has excellent reflow characteristics at low temperatures, and perhaps most importantly, the resolution capability of this photoresist is about 1 μm for thin deposits.

Development of the exposed resist is carried out using Microposit MF-319, which is a TMAH based developer designed for this purpose. The manufacturer's characterization of the spin speed versus film thickness of this photoresist was available for an 8" wafer. Since 4" wafers were used in this work, a re-characterization of the spin speed versus film thickness was performed as shown in Figure 7-1. It can be seen that

thickness ranging from 6 μm to 40 μm can be achieved using one coating of the photoresist. The range of achievable thicknesses spanned the feature sizes of the designed interconnect, and hence only one type of photoresist was used in the fabrication of the 200 μm pitch Delta interconnects.

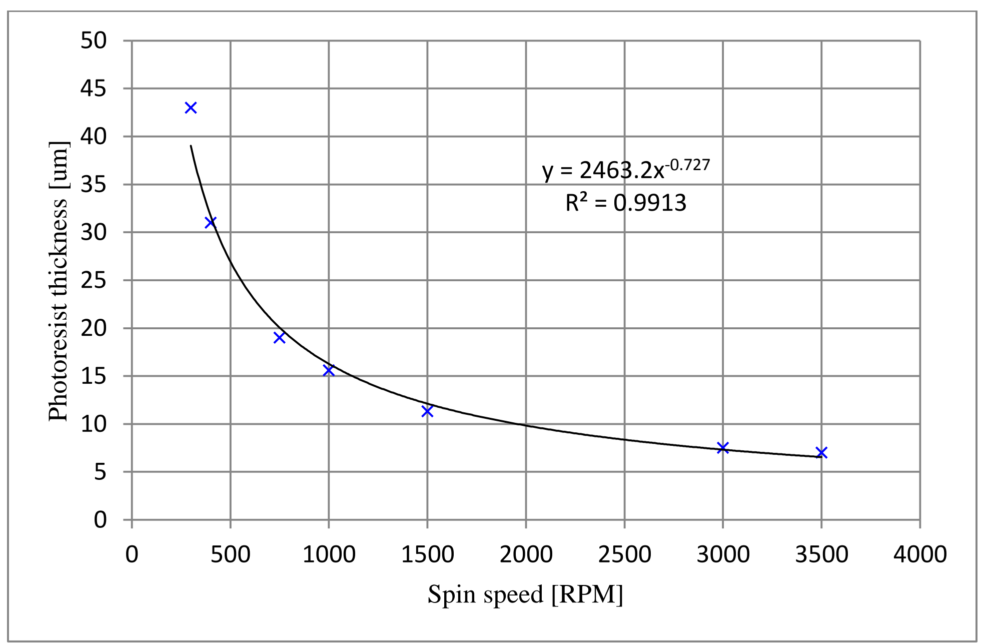


Figure 7-1: SPR220-7 film thickness vs Spin speed curves for a 4" wafer

Figure 7-2 shows the absorbance curves of exposed (lower curve) and unexposed SPR220. While SPR220 is an *i*-line (365 nm wavelength) capable resist, the curves show that the *h*-line (405 nm wavelength) absorption is greater than the *i*-line by about 30%. Based on this observation, 405 nm wavelengths were used for this fabrication. Finer wavelengths are used to obtain better resolution particularly for very fine features. Since the minimum feature size in this fabrication was 6 μm, the use of a slightly longer wavelength for exposure worked very well.

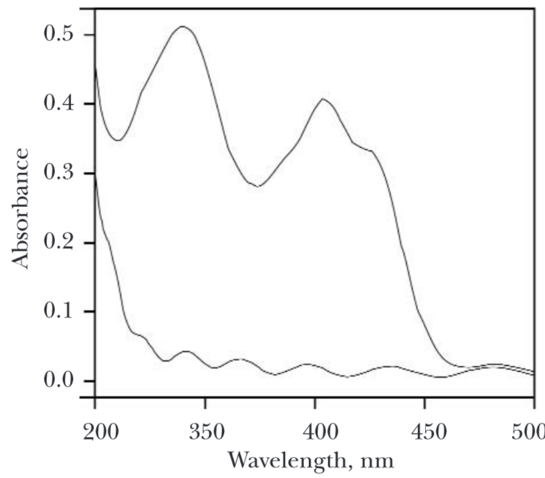


Figure 7-2: Absorbance curves of exposed (lower curve) and unexposed SPR220 [70]

7.3. MULTI-PATH INTERCONNECT FABRICATION

7.3.1. Mask Design

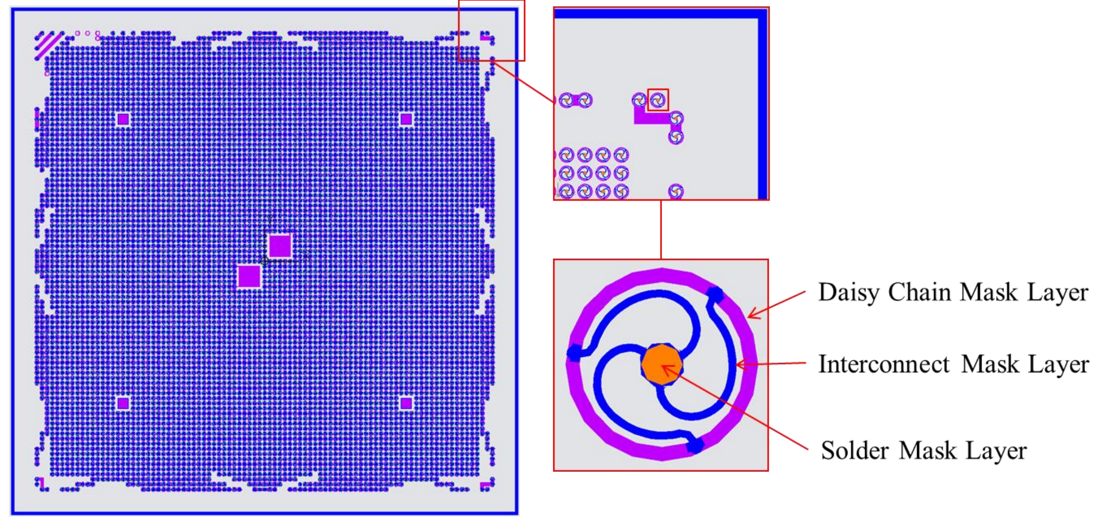


Figure 7-3: Die layout

Fabrication of the interconnects was carried out on 4” wafers. Over a 4” diameter, a total of twelve (12) 20 mm x 20 mm dies could be accommodated. Figure 7-3 illustrates the layout of one such die. A total of three masks were needed for the realization of the full structure. The first mask layer defines the Daisy chain structures, the second defines the interconnect, and the third defines the solder opening above the interconnect. Only the outer three rows of interconnects were Daisy chained for the

purposes of thermo-mechanical fatigue life monitoring based on observed failure locations in the models.

Based on the finite-element models, the designed width of interconnects was 6 μm. However, with the realization that copper seed layers would be used in the fabrication of the interconnects (which would eventually be etched away during the release step) measures were therefore taken to ensure that the widths of the interconnects after fabrication were about the designed dimensions. To achieve the designed widths with respect to the fabricated samples, allowances were made to the arcuate beam widths to compensate for material loss during the release step. Fabrication of the interconnects described here incorporates two (2) seed layers: the first to build up the die pads, and the second for the build-up of the interconnects. During release, the stripping of the copper seed layers result in a thinning of the interconnect's dimensions. To make up for this loss, the interconnect's arcuate beam widths were increased by an additional 600 nm. Since there is technically no restriction in height, compensation for the thickness of the interconnect can simply be made up by plating beyond the designed beam thickness. Figure 7-4 is an image of an interconnect from the mask files with an updated width to compensate for etch losses.

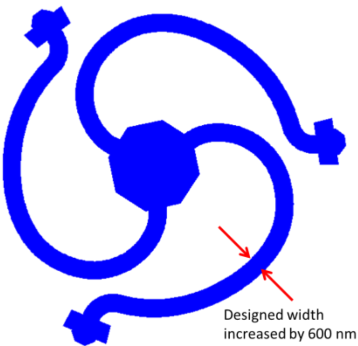


Figure 7-4: Interconnect mask width design increased to 6.6 μm to compensate for etch loss during release step

7.3.2. Process Overview

The fabrication steps for creating the interconnects is briefly summarized by the images in Figure 7-5. Starting with a wafer with annular pads and patterned resist, as illustrated in Figure 7-5a, the resist is reflowed in an oven (or on a hotplate) to generate the dome profile shown in Figure 7-5b. A metallization seed layer of titanium and copper (Figure 7-5c) is then sputtered over the wafer for electroplating the compliant structure.

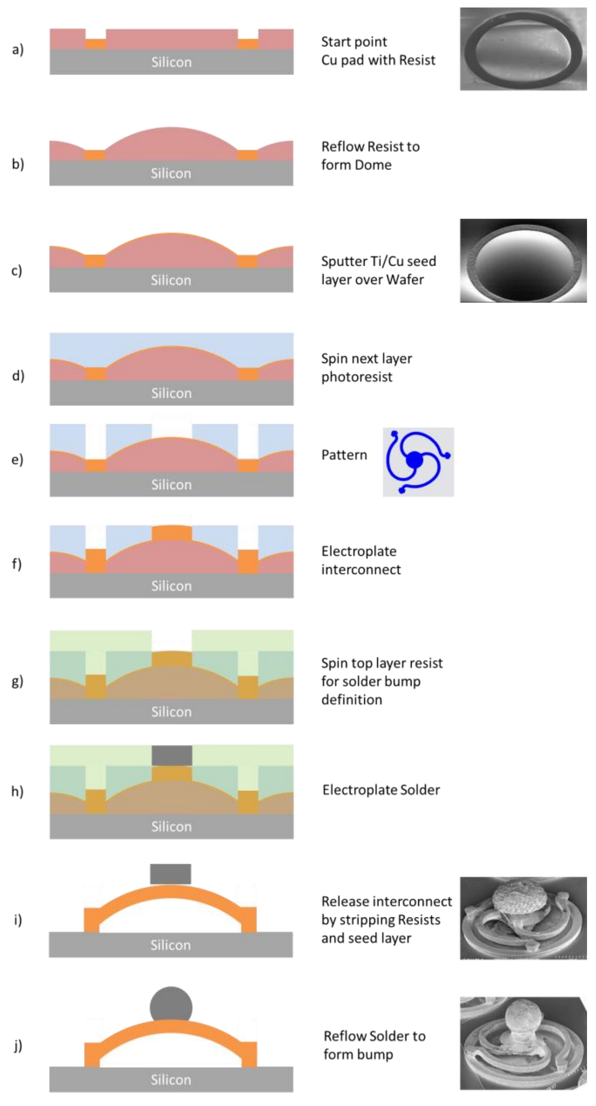


Figure 7-5: Fabrication of domed interconnects

The titanium layer ensures adhesion of the sputtered copper layer to the annular copper pad to improve its structural integrity. Following the metallization step, a second photoresist layer is spun onto the wafer as illustrated in Figure 7-5d for patterning the interconnect geometry. The photoresist is then patterned as in Figure 7-5e, and the interconnect plated up as in Figure 7-5f.

Upon completion of the interconnects electroplating step, a third layer of photoresist is spun to define the mold cavity for electroplating the solder as shown in Figure 7-5g. Solder is then electroplated as shown in Figure 7-5h. This completes the buildup process for the interconnects. The next step involved the release of the fabricated structures to make them free-standing. First, the top two resist layers is stripped away using an appropriate stripper, and then the copper/titanium seed layer is etched away using appropriate chemistries with good selectivity between copper and solder. This exposes the underlying polymer dome, which is then etched away to reveal the free standing structure shown in Figure 7-5i. The last step which is the reflow of the plated solder shown in Figure 7-5j is an optional step. Unlike stencil printed solders, plated solder has sufficient mechanical rigidity and will stay adhered to the pad without the need for reflowing. Figure 7-6 shows a Pro-Engineer®5.0 3D rendering of the finished fully released interconnect while Figure 7-7 shows the SEM image of fabricated interconnect without the plated solder. Various process steps are discussed in detail in subsequent sections.

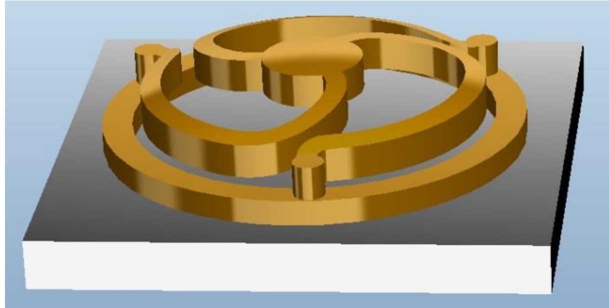


Figure 7-6: Pro-Engineer®5.0 3D rendering of Interconnect

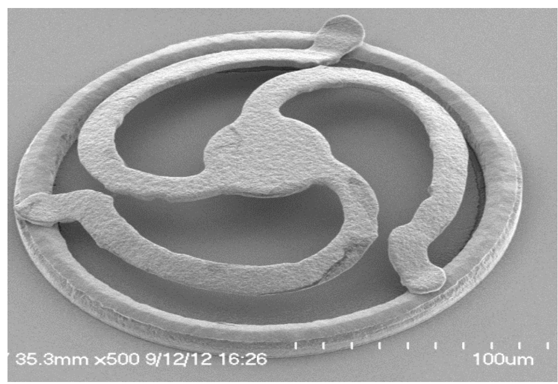


Figure 7-7: Fully released domed interconnect sample

7.3.3. Pad Fabrication

The copper pad on which the interconnects are to be fabricated is typically present at the end of wafer fab process. However, because this fabrication was carried out on a blank wafer, the pads were created first, before the commencement of interconnect fabrication.

The first step performed is a cleaning step. While the wafers used were vacuum packaged as shipped by the supplier, they still require cleaning, as failure to clean the wafers can result in loss of adhesion of the fabricated features. A simple solvent clean with each step lasting a few minutes is performed. The cleaning procedure calls for a sequential cleaning in acetone, methanol and isopropanol, followed by a rinse with deionized (DI) water. The wafer is then dried using a nitrogen gun to rid the sample of all visible droplets of water. This is followed by an oven bake at 150 ^{o}C for about 5 min. The bake step can also be performed on a hotplate.

The clean and dried wafer is then transferred to a sputtering chamber for the copper seed layer metallization. Copper by itself has poor adhesion to SiO_2 (native oxide on the silicon wafer). To enhance its adhesion strength, a thin layer of titanium was used as an adhesion promoter. The stability of the oxides produced by titanium gives it good adhesion to silicon. Being sputtered in an inert environment, a metallic bond is created

between the sputtered copper and the titanium, which firmly holds the copper layer to the silicon wafer. The thickness of titanium used is about 100 Å and sputtered at a rate of 75 Å/min. The copper seed layer which provides seed material on which electroplated deposits will grow is usually thicker to enable it to handle high plating currents during the electro-chemical deposition step. The seed layer thickness used is about 1500 Å and sputtered at a rate of about 800 Å/min.

The sputtering tool used for this fabrication is a UNIFILM® magnetron sputterer capable of achieving uniform deposits with a variation of less than 1 %. While the process is not particularly sensitive to small variations in film thickness, a uniform film reduces the risk of yield failures from regions with inadequate metallization. For sputtering tools with non-uniform deposits, a thicker adhesion layer is recommended.

Following the metallization of the wafer is the photoresist coating step. Prior to applying the photoresist, the wafer is placed on the wafer chuck of a spin coating machine and centered. Using a dropper, about 5 ml of SPR220 is deposited at the center of the wafer and then spun to give a uniform thickness polymer film. The desired pad thickness for this fabrication was about 10 µm. However, to accommodate the creation of the center dome, a 15 µm coat of photoresist was deposited. Based on the plot provided in Figure 7-1, the wafer was spun at 1000 rpm for a duration of 30 s.

After coating, the wafer was soft baked on a hotplate set at 110 ^{o}C for 100 s to drive-off the excess solvents in the photoresist. To prevent clumping up of the photoresist during the bake step, stepping of the wafer down to the hotplate to allow more gradual heat-up of the photoresist was employed. Large temperature gradients during the bake of thick photoresists agitate the photoresist, causing regions of the deposit to aggregate in lumps distorting the uniformity of the coat. Following the bake step, the wafer is allowed to cool before exposure to ultra-violet (UV) radiation. Photolithographic exposure of the sample to UV radiation with a wavelength of 405 nm was performed using a contact mask aligner manufactured by Karl Suss®. The exposure dose utilized was about 660

mJ/cm^2. Depending on the intensity of the light source, exposure time can vary greatly. While the manufacturer's recipe calls for a post exposure bake (PEB) step, this step was omitted, as the features were observed to develop satisfactorily without the PEB step. Furthermore, the PEB seemed to have a rounding effect on the edges of the patterned features which was considered undesirable.

Development of the exposed photoresist followed the exposure step. A period of about 30 mins was allowed to elapse between exposure and development to allow rehydration of the photoresist as called for by its data sheet. The rehydration step allows diffusion of atmospheric moisture into the wafer to complete the photochemical reaction. The developer solution used was MF319™ manufactured by Micro Chem. The wafer was developed in a bath of MF319 with periodic agitation to replenish used up reactants in the vicinity of the features. The development time lasted about 4 minutes. After development, the wafer was thoroughly rinsed in DI water and then dried using a nitrogen gun. Figure 7-8 shows an SEM image of pad openings prior to electroplating.

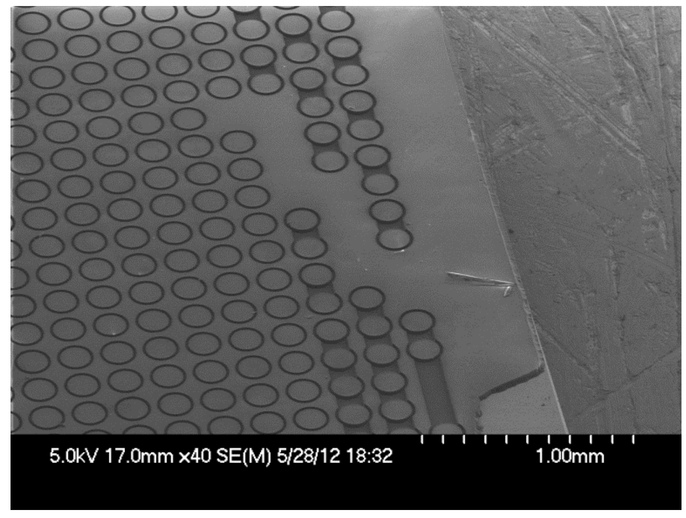


Figure 7-8: Image of developed photoresist showing pad openings

Following development, the wafer is descummed for 30 s using oxygen plasma. While this step is an optional fabrication step, it is performed to increase the surface energy of the photoresist. After development and rinse, the photoresist exhibits

hydrophobicity which causes it to repel water from its surface. The descum process (or more appropriately O_2 plasma treatment) is used to change the behavior of the photoresist from being hydrophobic to hydrophilic by implanting O_2 molecules into the resists surface. This ensures that during the electroplating the micro-cavities created through photolithography will be filled with electrolyte, thereby avoiding air locks. Air locks are common and result in yield failures when features do not plate as a result of not being in contact with the plating solution. An alternative method of avoiding an airlock condition is by rinsing the wafer in DI water treated with surfactants prior to immersion in the plating bath. The surfactant used as an alternative method to avoid air lock conditions was Triton X100, mixed to a ratio of about 500 parts per million.

7.3.4. Electrolytic Copper Deposition

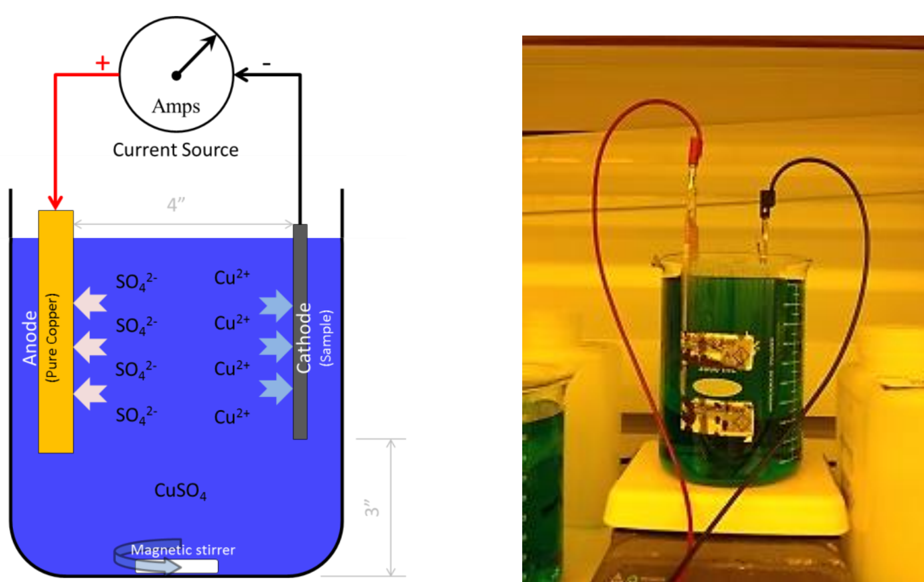


Figure 7-9: Copper plating bath setup

Electro-chemical deposition of copper was performed using a copper sulfate based plating bath. A typical plating setup is depicted in Figure 7-9. The plating bath setup included a 2 liter glass beaker (shown on the right), a teflon coated magnetic

stirring rod and magnetic stirring hotplate, current source, copper anode (metal source), and the sample to be plated which makes up the cathode. The current source used had the capability to supply direct or pulsating direct current depending on the attributes desired in the electroplated features. For this fabrication, direct current was used and plating was performed at constant current. When the circuit is closed, the application of current causes the electrolysis of the plating bath. When this happens, the dissolved salts in the bath separate into metal ions (cations) and anions. The positive metal ions are then forced toward the cathode where they are deposited as copper on exposed copper surfaces of the sample. To maintain bath equilibrium, copper atoms from the anode are released into the electrolyte to neutralize the radical $SO4^{2-}$ ions floating in the solution, thereby completing the current loop.

As a result of the depletion of the reactants in the vicinity of the cathode, agitation of the plating bath is required to ensure that depleted reactants are replenished to ensure uniformity of the plated deposits. Agitation of the solution was enabled through magnetic coupling between the magnetic stirrer and the teflon coated magnetic stirring rod inserted into the plating bath. Excessive bath agitation, on the other hand should be avoided as it can lead to uneven deposits. Regions most bombarded by the plating solution tend to plate faster than other regions.

Other measures that were implemented to improve the uniformity of deposits across the wafer include the maximization of the separation between the wafer and the anode, ensuring parallelism between the wafer and anode such that a uniform electric field is created across the wafer, and elevation of the wafer/anode well above the agitation source to prevent the subjection of the lower parts of the wafer to turbulent flow.

The composition of the plating bath used is listed in Table 7-1. The bath recipe was provided by Technic™ and is designed for standard aspect ratio structures; i.e., aspect ratios less than 10. In addition to the Carrier, which helps ensure level deposits,

low current densities not exceeding 10 mA/cm^2 were used for the fabrication to ensure good quality deposits. The plating bath setup is illustrated in Figure 7-9.

Table 7-1: Constituents of copper sulfate plating bath per liter

Constituents	Volume [mL]	Percentage [%]
$CuSO_4.5H_2O$	278	27.8
H_2SO_4	120	12
HCl	0.13	0.013
Brightner	5	0.5
Carrier	5	0.5
DI water	592	59.2

Current densities used for fabrication ranged between 2.5 – 10 mA/cm^2. Using the published values from the TECHNIC brochure as guide, the corresponding plating rates for the given current density range varied from about 3.5 μm/hr to 14 μm/hr respectively. It was, however, observed that the plating quality deteriorated with increasing current densities and the best finishes were obtained in the lower current density ranges. The daisy chains/copper pads were plated in the higher current density ranges, as they are merely structural supports. The lower current densities were used for the active elements of the interconnect (the arcuate beams) to ensure low defect density components. Figure 7-10 shows an image of an electroplated daisy chain structure.

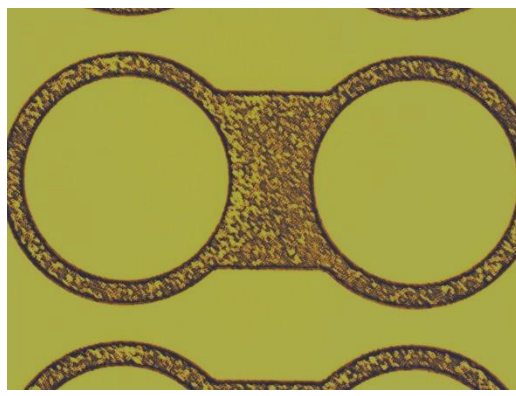


Figure 7-10: Optical image of plated daisy chain

7.3.5. Doming Process

Creation of the dome structures is an integral part of the dome mask design. To ensure that consistently uniform domes are created, the copper pads were designed of an annular nature to double as dams to confine the molten resist during reflow. However, to select an optimal reflow temperature, a reflow study was conducted on photoresists samples patterned in the form of discs. The samples were prepared by spinning SPR220 on a copper sputter wafer at 1500 RPM for 30 s. The samples were then baked and exposed accordingly. The height of the disks created were about 10 µm.

Table 7-2: SRP220 reflow study

	110 °C	115 °C	120 °C
Domes appeared dimpled			
	125 °C	130 °C	135 °C
130 °C appears optimal	Not performed		

The patterned samples were then baked on hotplate at the designated temperatures listed in Table 7-2 for a duration of 60 s. From the tables, samples that were heated below 125 °C showed some reflow activity, but the thermal energy was not enough to generate enough mobility in the photoresist to form perfect spherical dome sections. With the increase in reflow temperatures, samples baked at 130 °C and higher reflowed into perfect domes. However because the disks were not confined on these samples, the photoresists can be seen to spread beyond the initial disk radius. Based on this result, 130

^{o}C was chosen as the reflow temperature for the domes as it provided enough mobility in the resist to fully form domes and it also had a lower tendency to widen beyond its original area. Subsequent fabrications were thus reflowed at 130 ^{o}C. However, to ensure a more gradual heating of the samples, reflow is carried out in a convention oven at 130 ^{o}C for about 10 min. The longer bake time acts as a hard bake step to stabilize the photoresist against subsequent processing steps requiring heating.

It was observed, however, that there is a limiting photoresist disk height below which domes will not be formed. For the 200 µm pitch fabrication, it was observed that samples with disk outcrops of about 2 µm and less typically form domes with inverted peaks. In such cases, owing to the smaller volume of free resist, surface tension is not enough to overcome the attraction energy between the photoresist and the confining walls of the copper pads. Alternatively, if an undomed sample is desired, the reflow step is completely avoided. However, the hard bake step is still required, and is done at a lower temperature of about 60 ^{o}C for a duration of about 30 mins. Figure 7-11 shows a profilometer scan of the profile of a dome with an inverted peak.

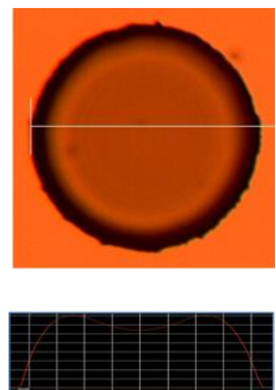


Figure 7-11: Profile of dome with an inverted peak

Following the reflow step is the metallization of the domed structures. Prior to metallizing the wafer, the oxides of copper built-up during the reflow of the photoresist is removed to improve adhesion of the next level metallization to the wafer. Sulfuric acid diluted to a ratio of 1:10 with DI water is used to etch built-up oxides on the copper pads.

This process is carried out for about a minute, after which the wafer is thoroughly rinsed in DI water and dried. Copper oxides form slowly at room temperature, nevertheless to ensure that the oxide levels are a minimum before metal deposition, the rinsing and drying of the wafer is done quickly and the wafer loaded into the sputtering tool's chamber. The presence of copper oxides compromises the structural integrity of the interconnect between the copper pads and the sputtered titanium layers which could eventually result in the delamination of plated interconnects as shown in Figure 7-12.

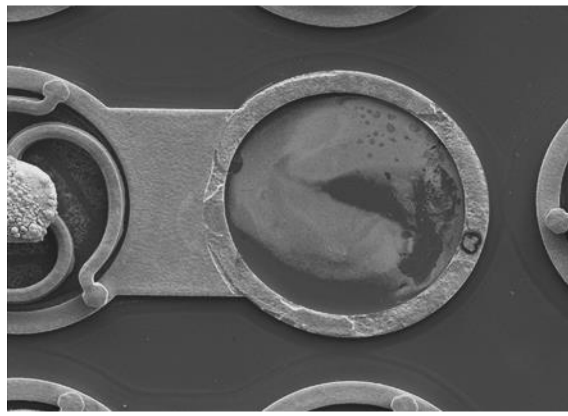


Figure 7-12: Interconnect delamination as a result of poor adhesion to copper pad

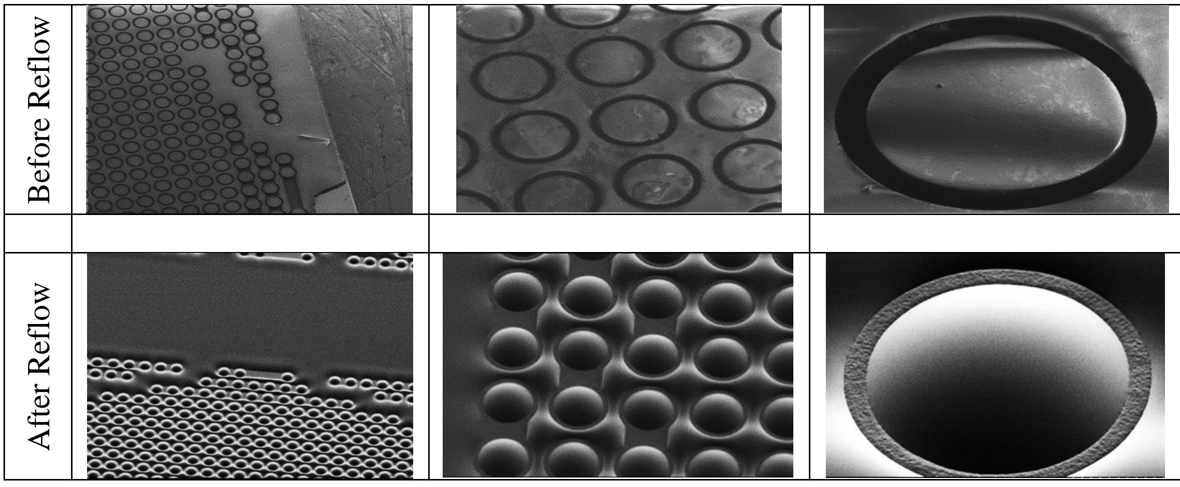


Figure 7-13: Polymer domes on daisy chains (metallized for SEM)

The wafer is then metallized using a sputtering process to create conformal coatings of titanium/copper over the domes. The total thickness of deposited titanium is about 100 Å followed by a 3000 Å thick copper seed layer. Figure 7-13 shows an SEM

image of metallized domes sitting in copper pads prior to the application of the third photoresist coating in which the interconnects will be defined.

7.3.6. Interconnect Layer Fabrication

With the first-level photoresist domed and metallized, the next layer of photoresist coating and development follows. The target thickness of plated interconnect for fabrication is about 13 μm. To create a photoresist coating thick enough to cover the 10 μm domes and yet provide enough depth to plated 13 μm of copper, at least a 23 μm thick resist coating is required above the copper pads. Shown in Figure 7-14 is a cross-section of a domed sample. Observations from numerous fabricated samples revealed that the dome height above the copper pads, b, is usually about twice the height of the surrounding resist above the copper pads, a. Hence, the free height of resist above the wafer needs to be about half the dome height plus the desired height of plated interconnect, d. Based on these numbers, a 19 μm photoresist coat was applied to the samples. To attain a 19 μm coating, the photoresist is spun at 750 rpm for 30 s and then baked in an oven set at 80 ^{o}C for about 40 mins. At such low spin speeds, if not controlled, the edge beads generated at such low speeds can be quite thick and interfere with alignment process. For ease of fabrication, it is recommended to remove the excess resist coalesced around the wafer edges.

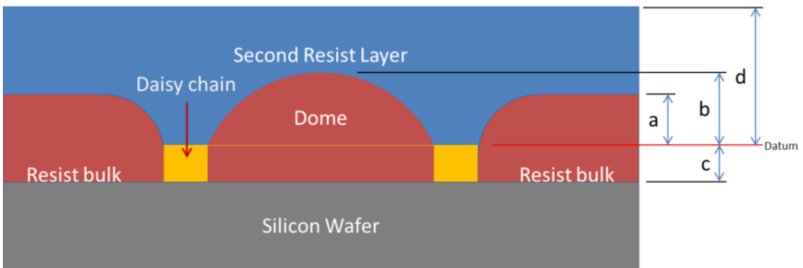


Figure 7-14: Cross-section of domes showing relative profile heights

The choice of a lower bake temperature and oven baking, as opposed to the use of hotplate, is to prevent the rupture of the metal dome caps concealing the supporting photoresist base. Photoresist has a much higher CTE than copper. With the metallization

of the reflow domes taking place at near room temperature, the baking of the metallization domes causes a build-up of pressure beneath the metal caps, as the photoresist expands at a greater rate than copper. At sufficiently high temperatures, enough pressure, if built-up beneath the photoresist, can rupture the domes as shown in Figure 7-15. To reduce the likelihood of such ruptures, the samples are hard-baked prior to metallization, and a thick seed layer (3000 Å) is used.

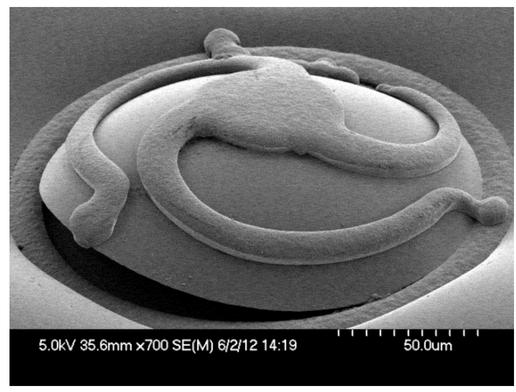


Figure 7-15: Ruptured dome as a result of excess pressures built-up beneath metal dome caps due to large thermal excursion of sample

Following the bake step, the wafer is exposed based on the deepest portion of the photoresist. Since the anchors/supports of the interconnects sit at the lowest levels, it is critical to ensure that these regions are well developed to ensure mechanical fastening of the interconnects to the pads. In this case, the exposure is calculated to the nominal resist thickness for the given spin speed to half the dome thickness. A relationship between photoresist thickness and exposure dose that was found to work for the fabrications in this work was 660 mJ of UV radiation for every 11 μm of photoresist. After exposure, the wafer is allowed to rehydrate for at least 2 hours before development. To ensure that all features are well developed, the samples are developed between 7 – 9 mins with optimal inspections performed closer to the end times.

The interconnects are plated next after a surface activation of the photoresist using O_2 plasma. The current density used for plating the interconnects is between 2.5 mA/cm^2

to 5 mA/cm^2 depending on fabrication conditions. At a rate of 7 μm/hr it takes roughly 2 hours to plate 13 μm at 5 mA/cm^2.

7.3.7. Solder Plating

The solder plating step is the last of the build-up process and is an optional step dependent on if the substrates to be assembled are pre-bumped. For electro-deposited solder, SPR220 is spun at 1500 RPM for 30 s at a ramp rate of 150 RPM/s, thereby creating a double coat of photoresist over the wafer. The slow ramp to the desired speed reduces the likelihood of trapped air within the trenches above the plated anchors of the interconnects.

After the coating step, the wafer is then baked at 80 ^{o}C for about 40 mins. Nominally, the coated resist height at 1500 RPM is about 10 μm. However, before the photoresist coat is now applied to a surface with similar characteristics, the interaction between the two coats usually results in an additional 5 μm of thickness. Hence, the exposure dose to define the solder openings is obtained by adding 5 μm to the expected photoresist thickness, in addition to deficit between the plated interconnects and the top of the second layer photoresist. The wafer is then allowed to rehydrate before development. After patterning, the wafer is O_2 plasma treated prior to plating to improve wetting. Before the electro-deposition of solder, copper columns about 10 μm tall are first plated to remove the soon-to-be-plated solder away from the arcuate beams of the interconnect as shown in Figure 7-16. This helps ensure that during reflow of the plated solder the arcuate beams will not get wetted by solder.

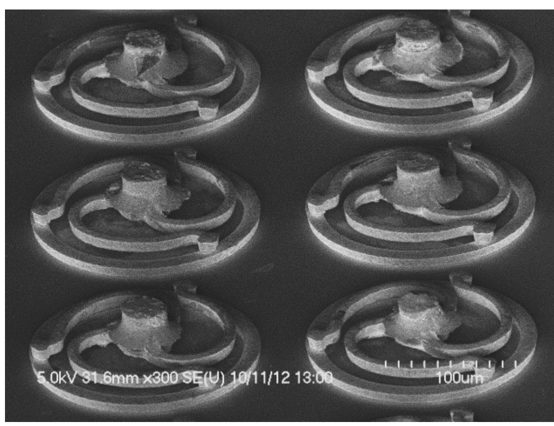


Figure 7-16: Interconnects with extended center pads to avoid wetting of interconnects during solder reflow or during assembly to bumped substrates

The solder plating solution used is a lead-free eutectic tin-silver solution manufactured by Technic©. The solution components were combined according to the ratios in Table 7-3. For assembly purposes, the lowest melting point alloy is desired, and hence a solution with the an eutectic amount of 3.5% silver or less is preferred, as the melting point of the alloy tends to be between 221 and 231 ^{o}C. The setup for electroplating tin-silver solder is identical to copper plating with the exception of the copper anode being replaced with a pure tin anode.

Table 7-3: Constituents of tin-silver plating bath per liter

Constituents	Volume [mL]	Percentage [%]
Technistan Ag Acid	85	8.5
Technistan Ag Tin Conc.	83	8.3
Technistan Ag Make Up	200	20
Technistan Ag Brightener	25	2.5
Technistan Ag Silver Conc.	7.5	0.75
DI water	balance	59.95

Unlike copper plating, tin-silver plating is performed at high current densities in the region of 50 mA/cm^2 to 300 mA/cm^2 for plating rates ranging between 2.15 µm/min to 5.8 µm/min. As a consequence of the high current densities, backside plating of the wafer with solder is not uncommon. To prevent this, a piece of blue tape is attached to the backside of the wafer prior to solder plating. For this fabrication, current densities

between 75 mA/cm^2 and 100 mA/cm^2 worked best. A challenge with the electrodeposited solder is the non-uniformity of the deposits. This was found to improve when the current density is about 100 mA/cm^2 and the solution is very gently agitated. Figure 7-17 is an image of fully released interconnects with electroplated solder.

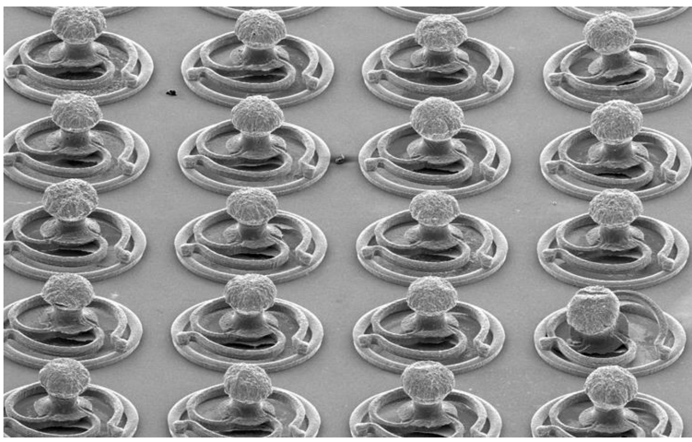
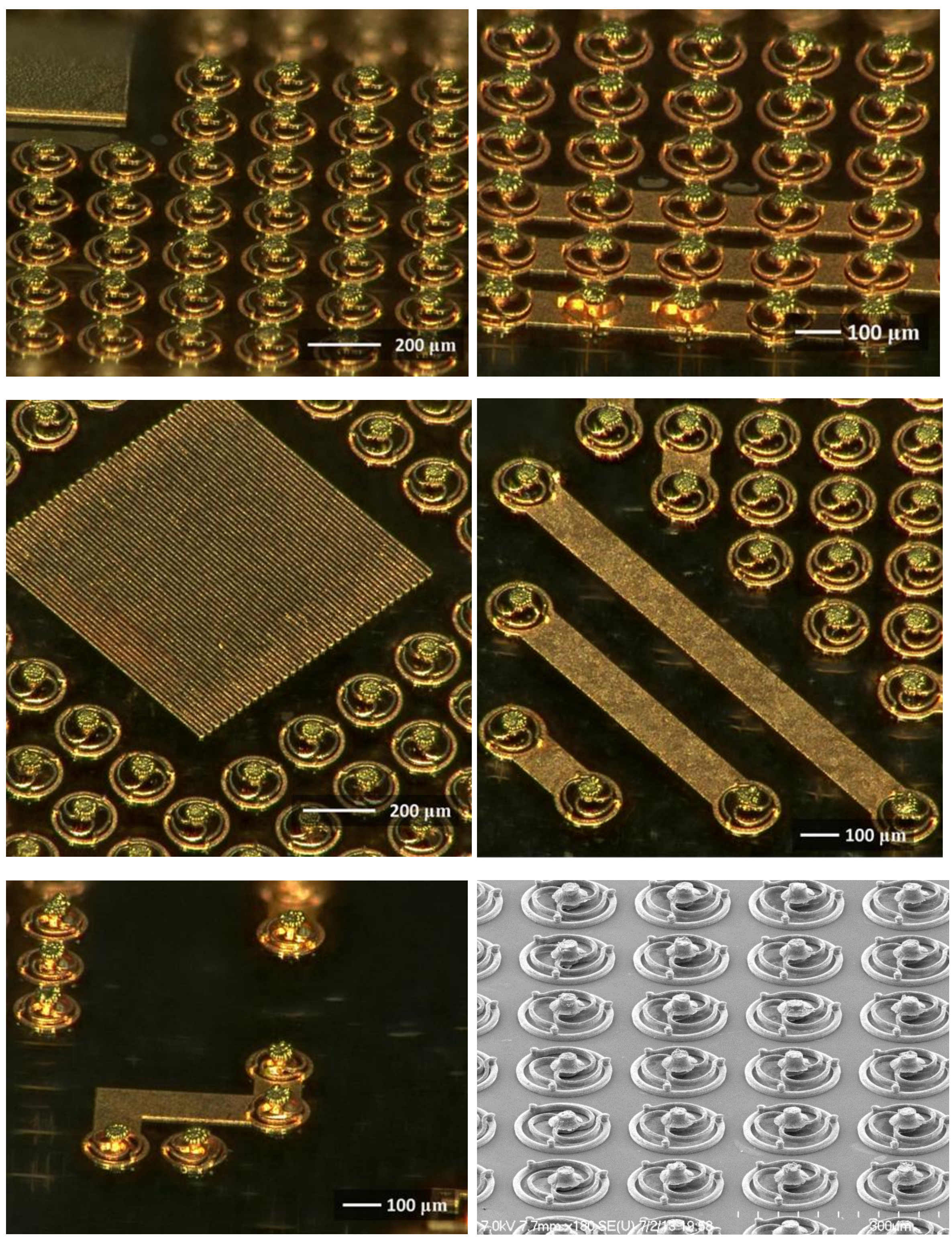


Figure 7-17: Interconnects with copper columns and plated solder

7.3.8. Release of Interconnects

The release of the interconnects is the last step in the fabrication process. In reverse order, the build-up layers are stripped using appropriate chemistries. Since this fabrication was done with positive photoresist, the interconnect and solder resist layers are flood exposed to UV radiation and the photoresist developed. The second copper seed layer is then etched away using a 2 mol solution of citric acid and hydrogen peroxide. The top adhesion is then exposed and is etched using buffered oxide etch. The first level photoresist now becomes visible and is stripped using acetone followed by a methanol, isopropanol and di water rinse before etching of the base seed layer. The bottom seed layer and adhesion layers are etched in the same way as the layers. Citric acid is used for the etching of the seed layers as it has good selectivity between copper and the plated solder. Etchants containing HNO_3 tend to attack solder rapidly and etch it away before the copper seed layer is completely etched. Hence, such solutions should be avoided

during release. Figure 7-18 is a gallery of images of released samples with and without electroplated solder caps.



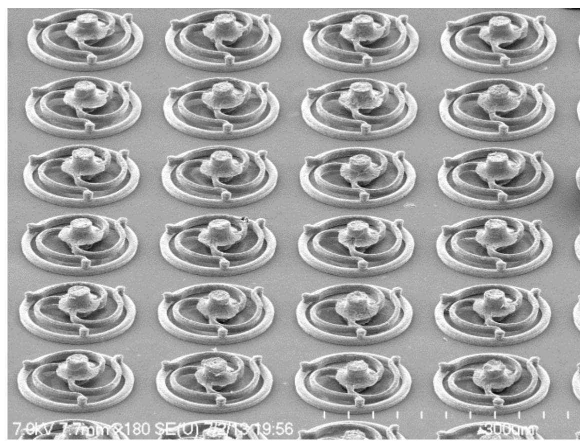
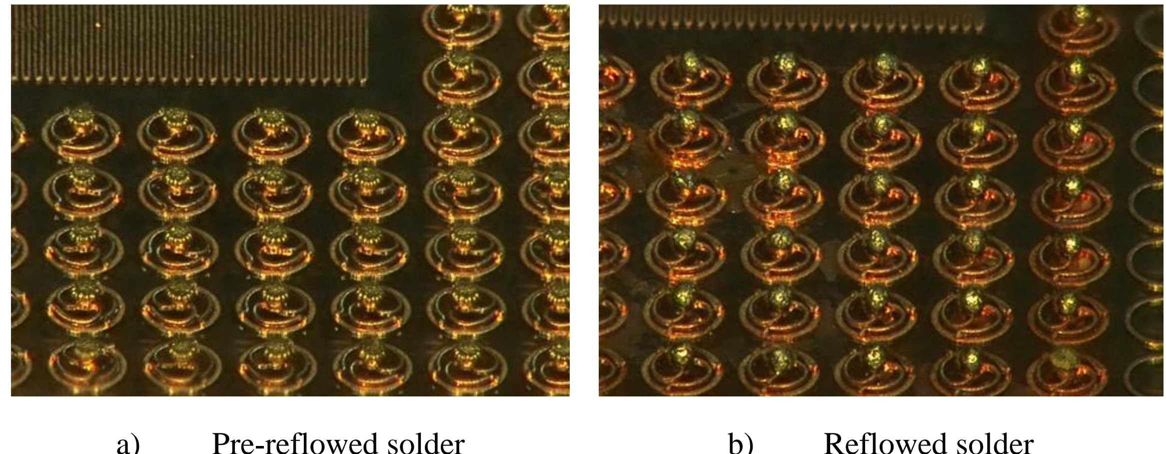


Figure 7-18: Images of released interconnect samples

7.3.9. Solder Reflow

Solder reflow prior to assembly is an optional step, as several samples were assembled without first reflowing the solder. The electroplated solder deposits have good mechanical strength and adhere well to the plated copper structures and do not need to be reflowed to improve their retention on the interconnects. However, reflowing the solder increases the stand-off height of the interconnect by turning the mushroomed plated solder into spheres as shown in Figure 7-19.



a) Pre-reflowed solder   b) Reflowed solder

Figure 7-19: Pre-reflowed and reflow solder bumps on compliant interconnects

To reflow, flux is first applied to the samples before immersion of the samples in an oven set to about 250 ^{o}C. Attempting to reflow without flux does not work well, as the

oxides accumulated on the surface of the solder prevent it from reflowing. With the application of flux, the surface oxides are removed during the activation of the flux and its continued presence creates an oxygen-free environment, enabling surface tension to pull together the deposited solder into spherical shapes.

CHAPTER 8

REFLOW OF ASSEMBLY DEVELOPMENT OF DELTA INTERCONNECTS ON ORGANIC SUBSTRATE

8.1. INTRODUCTION

The design of Delta interconnects has been discussed extensively, and through finite-element models, an understanding of the effects of geometric changes on its performance through parametric studies was gained. The selected design was a compromise between the thermo-mechanical fatigue life and the electrical resistance of the interconnect. Following the design process, photomasks were generated through an outside vendor for the fabrication of these interconnects. The fabrication process, which represents the transformation of the interconnect design into prototype, included several iterations in process design, each aimed at solving distinct challenges encountered in the build-up process. Finally, with these interconnects fabricated, assembly and testing can be performed to characterize the performance of these interconnects and provide validation for the prediction models. This chapter looks into the design of the test features on the die and organic substrate test vehicle. The assembly process, including assembly challenges encountered, will also be discussed.

8.2. SIGNIFICANCE

The assembly process represents the integration of a component item into a network or circuit to achieve a certain function. The component item could be a simple passive device, such as resistors, capacitors and inductors, or active components such as operational amplifiers or clocks/oscillators, to mention a few. In the case of this work, the component item is a dummy die with inbuilt daisy chain patterns specifically designed to aid in the assessment of the interconnect's performance.

Challenges were encountered during the assembly process, none of which is foreign to the standard flip-chip assembly process. Some of the concerns resulting from

the fabrication process could be a variation in the interconnect height due to uneven plating of the interconnects, or solder caps, or both. In either case, an uneven surface for assembly is presented, which could be further exacerbated by the non-planarity of the organic substrate. Methods of addressing such challenges include the use of thermo-compression bonding to keep the die flat on the substrate during the reflow step. Control of the applied load is critical, as too little may prove to be inadequate and too much could completely squish the reflowed solder, thereby creating a risk of wetting/fusing the interconnect's paths together.

Another challenge which other researchers in the field have experienced is the wetting of the unprotected surface of the copper structure. Molten solder, which has a high affinity for copper, wicks along the paths of the interconnect, fusing the interconnect with its central pad into a lump of metal. This condition destroys the compliance of the interconnect and completely alters its characteristics, both mechanically and electrically. The resulting interconnect assembly could potentially become much stiffer than a traditional solder bump, depending on the severity of the wetting. This work has employed copper oxidation as means to prevent over-wetting of the interconnects.

8.3. TEST VEHICLE DESIGN

The test vehicle used in this work was fabricated from an organic-based substrate manufactured by Isola®. The test vehicle consisted of a single level of metallization to enable routing of electrical signals and was designed to accommodate a 20 mm x 20 mm die with interconnects at a pitch of 200 µm. The substrate had a thickness of 500 µm with planar dimensions of 40 mm x 40 mm. The board was oversized to accommodate several electrical connection points for probing the built-in test features. Some of the test features incorporated into the board design include three (3) peripheral rows of daisy chained interconnects for thermo-mechanical reliability assessment, seven (7) four wire Kelvin structures, for accurate measurement of an individual interconnect's resistance and electrical test features for the determination of resistance, inductance and capacitance

through insertion loss measurements. Figure 8-1 is an illustration of the test vehicle highlighting some of its key features.

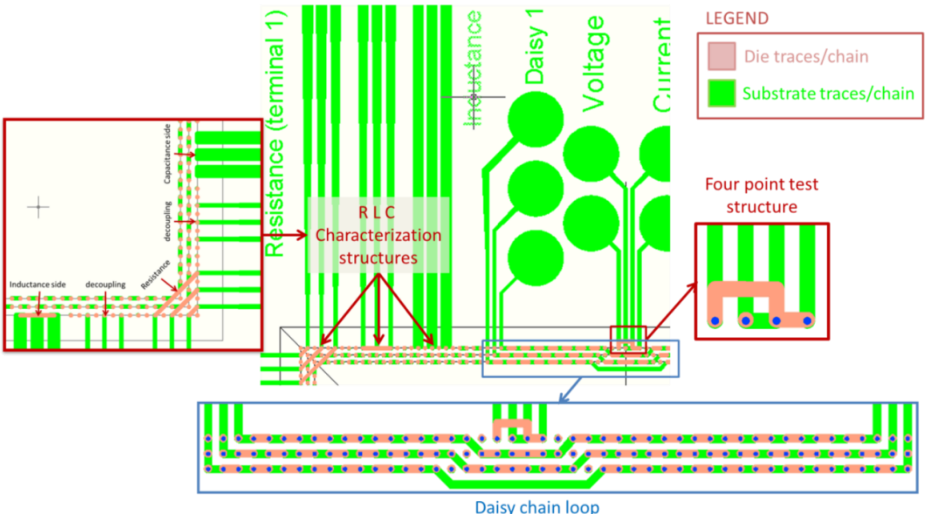


Figure 8-1: Highlight of features embedded in test vehicle design

8.4. THERMO-MECHANICAL RELIABILITY ASSESSMENT

Thermo-mechanical reliability performance assessment to ascertain the fatigue life of the interconnect was performed. To make it tractable, a failure metric was needed to determine when the interconnects were considered to have failed. The traditional method of checking interconnect failure is by measuring the path resistance of the associated interconnects through daisy chain loops. To implement this, daisy chains were incorporated into the test vehicle design with complementary pairs incorporated into the die such that a continuous electrical path is created through several interconnects. With the onset of fatigue, a micro-crack is formed within the interconnect's path or arcuate beam and continues to propagate with further thermal cycling until the path is severed, which in turn will be observed as an increase in resistance. Since the interconnect is of a multipath design of order 3, the failure of one of its paths only increases its resistance by 50%. Depending on the sensitivity of the probing multi-meter, this change might be undetectable particularly in a long daisy chain. To enable tracking of the interconnect's

change in resistance with the progression of damage, four-wire test structures were inserted at the corners and mid-regions of the outermost row of daisy chain. With the greatly enhanced sensitivity of a four-wire resistance measurement by excluding the resistance of the leads, change in interconnect resistance could easily be observed. Figure 8-1 shows an insert of a daisy chain segment with three parallel loops corresponding to the three (3) outermost interconnect rows. The rose colored traces represent die traces while the green colored traces belong to the substrate.

Figure 8-2 shows an image of the 200 µm pitch test vehicle design used primarily in this work. The daisy chain loops monitoring the three (3) outermost rows of interconnect were sub-divided into seven (7) segments. The longest chain, which encompasses an angle of almost 360 degrees, allows a single point measurement for the entire loop and is indicated by large blue arrows. However, in the case of failure as a result of thermo-mechanical fatigue or from defects during fabrication, intermediate probing points (indicated by the smaller arrows) were also included to localize the failure of the interconnect to either the edges or the corners of the die. In addition to the daisy chain loops, four wire resistance measurement structures were positioned at critical locations, namely, the middle of the outermost row of interconnects and at the corners of the die to monitor single interconnects in these regions. The benefits are two-fold: first, the Kelvin structures can be used to accurately determine the resistance of individual interconnects for characterization purposes. Second, it enables accurate monitoring of the two critical regions in the die, and allows insight into the change in resistance of a single interconnect as a function of thermo-mechanical cycling.

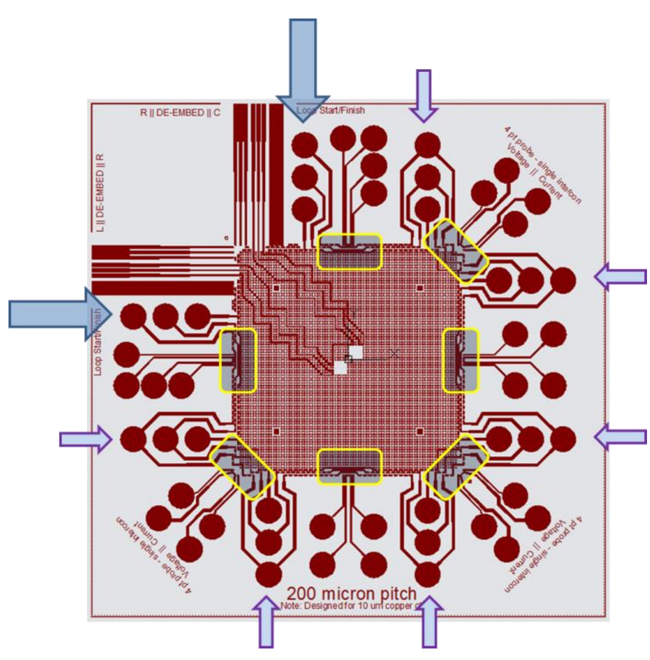


Figure 8-2: Test vehicle layout highlighting probing locations

8.5. SUBSTRATE FABRICATION

The test vehicle for the 200 µm pitch interconnect's were fabricated in-house using the Packaging Research Center's (PRC) next-generation substrate lab. Fabrication began with a pristine double sided copper clad FR4 board. The boards were cut down to 6" x 6" and laminated on both sides with a dry film negative photoresist at a temperature 120 °C. The photoresist used for this fabrication was FX920 manufactured by Dupont®. The nominal thickness of the photoresist is about 20 µm after lamination. For intricate designs, such as patterns with fine pitches, thin photoresists such as FX920 give better pattern transfers. Using photolithography, the trace patterns imprinted on the film mask were then transferred to the photoresist. The mask pattern used is the inverse image of Figure 8-2 since the fabrication employed a negative photoresist.

The exposure step was followed by the development step, which utilized a spray developer. The developer solution was composed of calcium carbonate salts and deionized water and was sprayed against the samples as they traveled past the spray

nozzles on a conveyor. The developed samples were then run through an etcher to etch the copper in the developed regions, leaving behind the trace patterns protected by the photoresist. The copper etchant solution used for this fabrication was composed of copper chloride salts, hydrochloric acid, and deionized water in a ratio of 7:1:2 by volume respectively.

Using a photoresist stripper (Dupont EKC technology), the protective resist film over the copper traces was stripped away. The boards were then rinsed thoroughly with deionized water and oven dried in an inert atmosphere to prevent oxidation of the traces. Next, a photo-definable solder masking material was stencil printed on the board and baked to dry in a nitrogen oven at 140 ^{o}C for about 30 mins. Following the cure of the solder mask, copper pad openings were then defined by exposing the board to a collimated UV light source. A film mask with imprints of the solder mask openings was positioned over the substrate pads and exposed. The solder mask was then developed to expose the contact pads.

8.6. ASSEMBLY PROCESS DEVELOPMENT

The assembly process is representative of physically attaching a die to substrate to enable electrical communication between the die and the system. Using the Finetech® flip-chip bonder shown in Figure 8-3, the die was picked and then aligned with the substrate pads and then placed on the substrate. The tool is capable of submicron alignment accuracy, which makes it relatively easy to align the 200 μm pitch interconnects. A low-solids no-clean flux manufactured by Kester® (Kester 951) was then applied to the substrate, and its volatile contents were allowed to evaporate prior to die placement. Owing to non-uniformities in the plated solder heights, a thermo-compression bonding process was utilized for most assemblies. The applied force was removed just before the end of the dwell step at the peak temperature shown in the reflow profile in Figure 8-5. Removal of the assembly force allows the self-aligning characteristics of

solder to correct slight misalignments that may have been introduced during the alignment and placement steps. Figure 8-4 shows a placed die on the substrate prior to the commencement of bonding.

Figure 8-3: Finetech flip-chip bonder

To increase the likelihood of a successful assembly, some factors were considered during the assembly step. These factors include the surface finish of the copper pads, the type of flux used, the amount of compression load applied, the reflow temperature profile, and substrate fabrication.

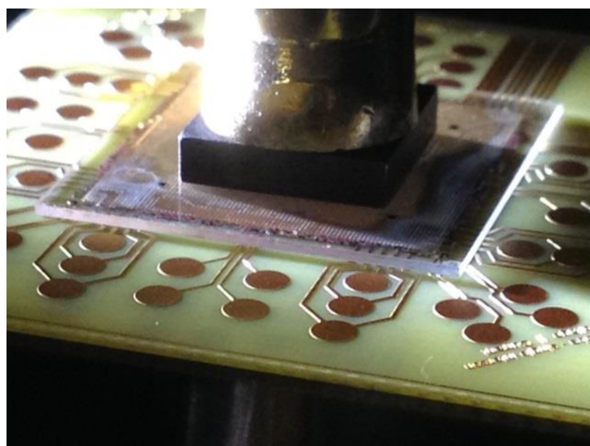


Figure 8-4: Placed die prior to assembly reflow

8.6.1. Substrate Pad Surface Treatment

Traditionally, contact pads on most substrate designs comprise a number of metallization layers serving a number of purposes. Depending on the application, surface treatments of the contact pad could be organic solder preservative (OSP), electroless-nickel immersion gold (ENIG) or electroless-nickel electroless palladium immersion gold (ENEPIG) to mention a few. The primary aim of the surface finish is to prevent the oxidation of the pads. Other functions include acting as a barrier layer to prevent the diffusion of the base copper metal into the solder bump formed on top of it during assembly. These surface finishes are crucial to the reliability of assemblies. An oxidized copper pad can lead to weak solder joints and could prevent wetting of the pad thereby creating an open.

In this work, however, as a result of the low volume of samples that were processed, a majority of the fabricated substrates had no surface finishes applied. To rid the sample of oxides prior to assembly, these samples were typically micro-etched in dilute H_2SO_4 solutions, and then rinsed with deionized water and blow dried prior to assembly. To prevent oxidation, a few drops of the liquid flux are applied to the substrate prior to assembly.

Surface finishing was of little interest because thermo-mechanical reliability simulations showed that failure of the interconnects will occur along its arcuate beams and not in the solder. Furthermore, an investigation of the reaction forces at the base of the interconnects show these forces are too weak to generate and/or propagate a crack through the intermetallics that form at the interface of solder and copper.

However, later fabricated boards were finished with a coating of ENIG. These boards were fabricated to trouble-shoot the cause of several failed assemblies to determine if the surface finish of the pads was the cause. The benefits of the ENIG finish helps prevent pad oxidation and allows rework of partial assemblies.

8.6.2. Flux

Two types of flux were used in the assembly: a tacky liquid flux and a low viscosity flux, both manufactured by Kester. A benefit of the viscous flux is that it helps retain the die in position on the substrate due to its tackiness. This could be useful if a pick and place machine was used to assemble the components, and reflow of the assembly was to be carried out in a remotely located oven. However, challenges encountered with the viscous flux came from controlling the quantity of flux dispensed. Too little flux might result in unprotected copper pads, and too much flux resulted in a build-up of pressure beneath the die, which, if no downward force was applied to the die could result in the die being thrown off the substrate.

The thinner flux was easier to use as a successful assembly was not dependent on a carefully controlled application of flux. However, unlike the viscous flux, the thinner flux does not temporarily secure the die to the substrate and may not work well for a pick-and-place type scenario.

8.6.3. Compression Load

Assembly of the interconnects does not require compression loading. The flip-chip bonder is merely utilized as a pick-and-place machine. Following the alignment step between the die and the substrate, the die is placed over the substrate and heating is commenced. With the standoff heights of the plated interconnects being within about 10% of each other, assembly should proceed without issues. Furthermore, because the die is not attached to the load head of the flip-chip bonder, the self-alignment action of the solder generated by surface tension of the melt helps correct minor placement offsets.

In a case where there is irregularity in the height of the plated solder, thermo-compression bonding is required. To avoid squashing of the reflowed bumps, a small applied load was selected for this process. The applied load was based on the compliance of the interconnects. For each of the fabricated die types, a load capable of compressing the interconnects on the die by about 2 μm was selected. It is believed that any deflection

less than 2 μm falls within the uncertainty of the measured compliance and that of the applied force. The measured compliance of the interconnect was 5 mm/N. For assemblies with full area array layout, a total of 8281 interconnects were present which translates to a compression load of about 3.8 N.

8.6.4. Temperature Profile

The temperature profile used for assembly is based off of JEDEC J-STD-020D. The maximum ramp up rate called for by this standard is 3 ^{o}C /s and a maximum ramp down rate of 6 ^{o}C /s. The peak activation temperature for lead-free based assemblies was 150 ^{o}C and the peak profile temperature was not to exceed 260 ^{o}C. In this work, however, because of the relative size of the heating head (10 mm) to the die (20 mm) as shown in Figure 8-4, only bottom heating was used for assembly.

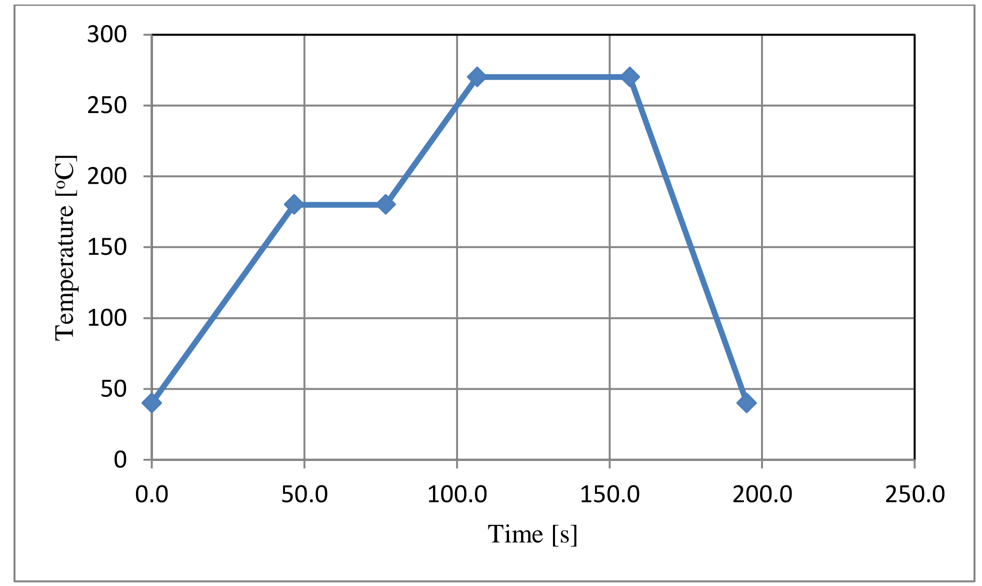


Figure 8-5: Reflow temperature profile used for assembly

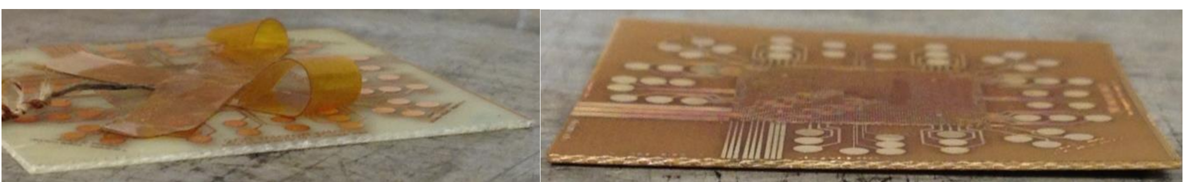
Temperature measurements performed on top of the substrate during a heat up cycle showed as much as a 25 ^{o}C difference between the measured and indicated temperatures by the chip bonder. For this reason, the temperatures selected for the soak and peak temperatures were augmented to account for this discrepancy. This led to the selection of a soak temperature of about 180 ^{o}C for a duration of 30 s for the dry out and

activation of the flux. The peak temperature selected was about 280 ^{o}C. Figure 8-5 is an illustration of the reflow profile input into the Finetech flip-chip bonder for assembly purposes.

8.6.5. Substrate Fabrication Considerations

Two types of test vehicles were fabricated in this work. The first was designed for assemblies undergoing thermal cycling while the second was for assemblies requiring electrical characterization in particular, scattering parameter measurements.

The test vehicles fabricated for thermal cycling had both sides of the substrate patterned with the daisy chains and traces. This ensured that the total volume of copper on both sides of the substrate was identical. The need for a balanced copper distribution across the substrate comes from the CTE mismatch between copper and the FR4 material of which the substrate's core is made. The core CTE is 11 ppm/K below its glass transition temperature and 13 ppm/K above it. In either case, its CTE is lower than that of copper, which has a CTE of 17.3 ppm/K.



Balanced substrate at 220 ^{o}C　　　Substrate with ground plane at 220 ^{o}C

Figure 8-6: Warpage comparison at solder reflow temperature between a balanced (left) and imbalanced copper substrates

. This creates a non-uniform distribution of copper across the substrate and leads to warpage of the substrate during assembly. The severity of the CTE mismatch between the core and copper, the percentage of volume mismatch, and the thickness of the copper clads relative to the core thickness all affect the degree to which the substrate warps. Initially fabricated boards had a core thickness of 500 μm and a 38 μm thick copper

ground plane. Assembly of this board proved to be a challenge as a result of the severity of the warpage as shown in right image of Figure 8-6. To lessen the likelihood of warpage, laminate boards with half as much copper were ordered, which greatly lowered warpage and allowed assembly of the electrical test dies. Likewise, a thicker substrate core improves the stiffness of the substrate, making it less likely to be bowed by the higher CTE copper beneath it. Since the samples undergoing thermal cycling did not require a ground plane, balancing the copper across the substrate allowed the substrates to remain flat during heating to the reflow temperature.

In order to create test vehicles for the electrical characterization of the interconnects, some modifications to its original design specifications were made. The original design called for a substrate core with a thickness of 230 μm with copper traces that there 45 μm thick. Under such configuration, the warpage of the test vehicle became excessive making assembly impossible. To enable assembly, the copper traces were cut down to 18 μm in thickness and the substrate core doubled to about 500 μm. The electrical test vehicle required a ground plane on the back side of the substrate to help confine electromagnetic waves around the signal lines during testing. This required the copper on the back side of the substrate intact to create a uniform plane. For such a configuration, warpage of the substrate during heating becomes very likely, depending on the severity of the CTE mismatch between the core material and copper, the percentage of volume mismatch between the top side and back side copper, and the thickness of the copper clads relative to the core thickness. Usually, the lower the imbalance of copper across the substrate, the lower is the substrate's warpage. Likewise, a thicker substrate core improves the stiffness of the substrate making it less likely to be bowed by the higher CTE copper beneath it. Since the samples undergoing thermal cycling did not require a ground plane, balancing the copper across the substrate allowed the substrates to remain flat during heat up to and cool down from reflow temperatures as shown in the right image of Figure 8-6.

8.7. ASSEMBLY YIELD CHALLENGES AND PROCESS ENHANCEMENT

During the course of assembling several samples, numerous failures were observed, and some of the identified causes of failure include defective samples, unconnected solder resulting from uneven height or the presence of foreign object between die and substrate, damaged interconnects, misaligned die to substrate pads and load head not parallel with substrate during assembly.

8.7.1. Defective Sample

The first failure type arises from defects stemming from the fabrication of the sample. Discussed under Section 3.1. is the failure of interconnects by delamination as a result of poor adhesion to the copper pads. If such a sample did not fail during the release step or during the dicing process where high pressure water jets are used to clear the churned out debris, then the next likely point of failure will be during the reflow cool down step.

Figure 8-7 is an exhibition/trouble-shooting sample of the interconnects fabricated on glass wafers. The glass dies were created to allow observation of the interconnects in the assembled configuration, and this greatly aided the trouble-shooting process. For example such failures as depicted in Figure 8-7 would not be readily observed if the die were to be made of silicon. This is evidenced by the greying of the ENIG coated pads as a result of solder wetting. Failure of this sample most likely occurred during the cool down to room temperature, as the assembled Delta interconnects can be seen to remain on the copper pads, while their bases are completely sheared off from the annular die pads. This suggests that there was very little traction between the interconnect and the die pad prior to assembly, and this readily gave way when thermally-induced loads were applied to the interconnect.

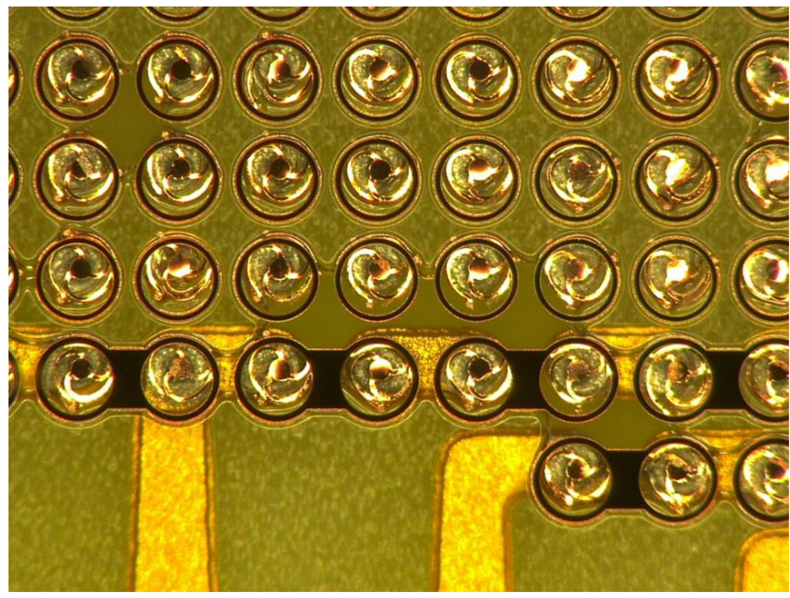


Figure 8-7: Sheared off interconnects after assembly reflow cool down as a result of poor adhesion

8.7.2. Non-uniform Solder Height

Perhaps the most prevalent failure based on observation was due to uneven heights of the plated solder. Figure 8-8 shows a profile scan of a sample's surface after the completion of the solder electro-plating step. Figure 8-8 shows the center solder being at least 3 times the height of the nominal thickness of plated solder. In such a case, this creates a stand-off between the surrounding interconnects and the substrate pads during assembly. This creates assembly failures like in Figure 8-9. Based on optical inspection of the sample, an entire edge of the die had no electrical continuity after assembly. The optical image also shows that there was no wetting of the substrate pads, suggesting no contact between the interconnects and the substrate. For less severe cases of overplating, an attempt at rectifying this problem is through thermo-compression bonding with long dwells at peak reflow temperatures to help disperse some of the excess solder onto the substrate pads.

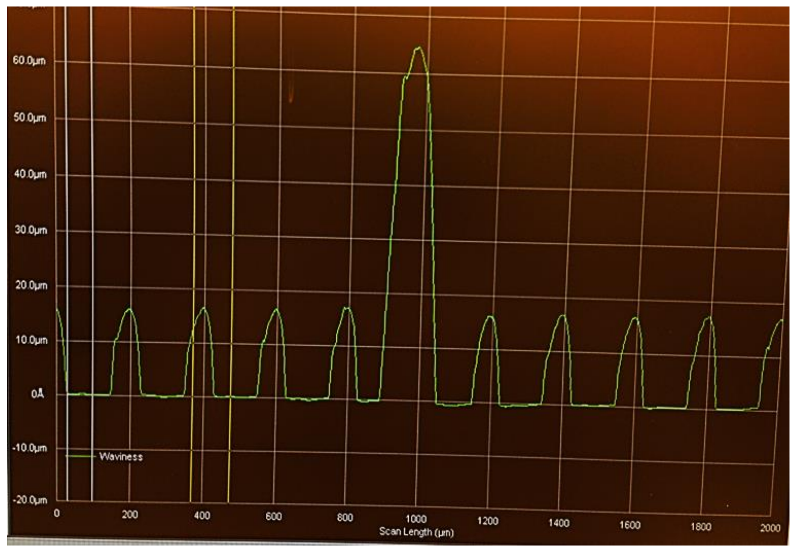


Figure 8-8: Grossly overplated solder creating non-uniformity in overall interconnect heights

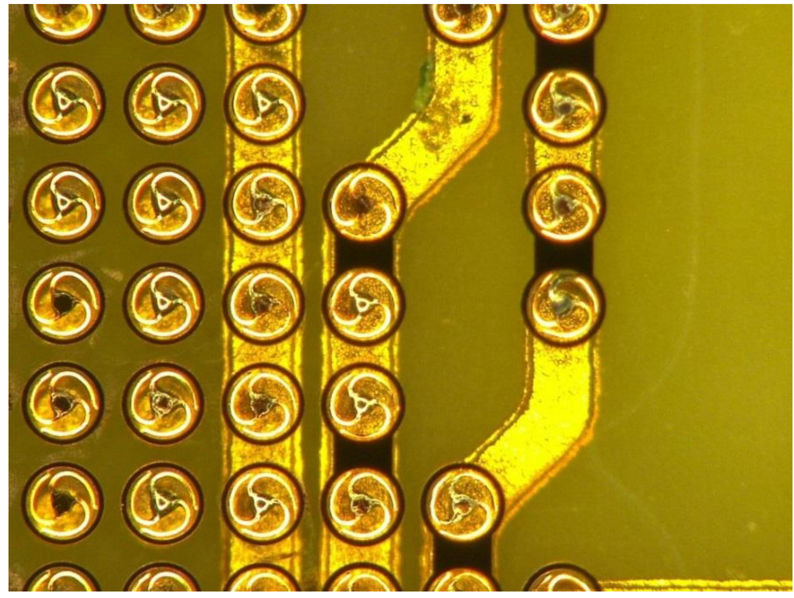


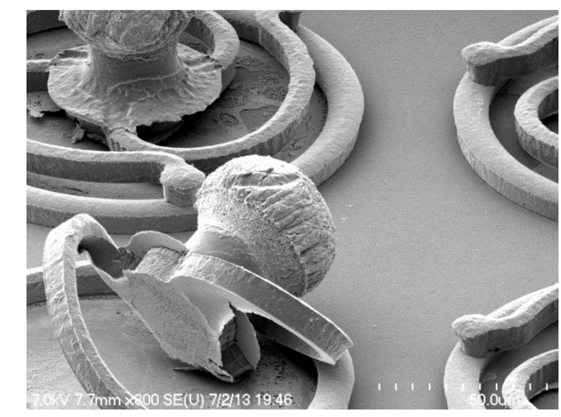
Figure 8-9: Edge of die showing no wetting of the substrate pads as a result of non-contact between interconnects and substrate pads

8.7.3. Damaged Interconnects

Damaged interconnects in the path of any daisy chain structure results in a continuity failure of the daisy chain after assembly. The impact of such failures is significant on long chains, as it can render an entire edge of the assembly die in active even though 99% of the interconnects assembled correctly. Figure 8-10a shows one such

damage resulting from poor handling of the released dies. In this case, the interconnect is deformed past the location of the substrate pad and according to Figure 8-10b, this can results in an open of such a connection. Other factors that could result in deformed interconnects are direct blasts of high pressure jets of water or air during the rinse and drying of the newly released structures. Subsequent die handling techniques were improved upon to minimize damage to the interconnects.

In cases where the deformity leaves the solder tip of the interconnect within the vicinity of the substrate pad, assembly is possible and continuity of the daisy chain will be registered upon assembly. However, as shown in Figure 8-10a under thermal cycling conditions, the deformed shape of the interconnect can result in premature failure of the daisy chain on which it is located. This can lead to false conclusions that the fatigue life of the interconnects are relatively short, but in reality, these are infant mortality failures.

a) 

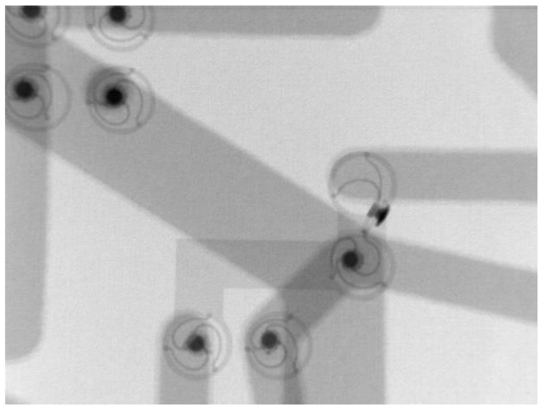
b) 

Figure 8-10: Image of damaged interconnects caused handling errors a) SEM pre-assembly micrograph b) X-ray inspected sample post assembly

8.7.4. Misaligned Pads

Another failure type observed involved the misalignment of the interconnects from the substrate pads. This was by far the least prevalent failure type observed. With regard to the imaged samples shown in Figure 8-11, the assembly was performed with excess tacky flux with the vacuum on the chuck turned off. Upon attaining sufficiently high temperatures, the boiling of the flux caused a shift in the die resulting in the misaligned pads shown. The red arrows in Figure 8-11a point to the direction the solder

at the arrow ends need to move to align with the substrate pads. Figure 8-11b shows an angled view of another region of the assembly revealing the offset between the solder and copper pads.

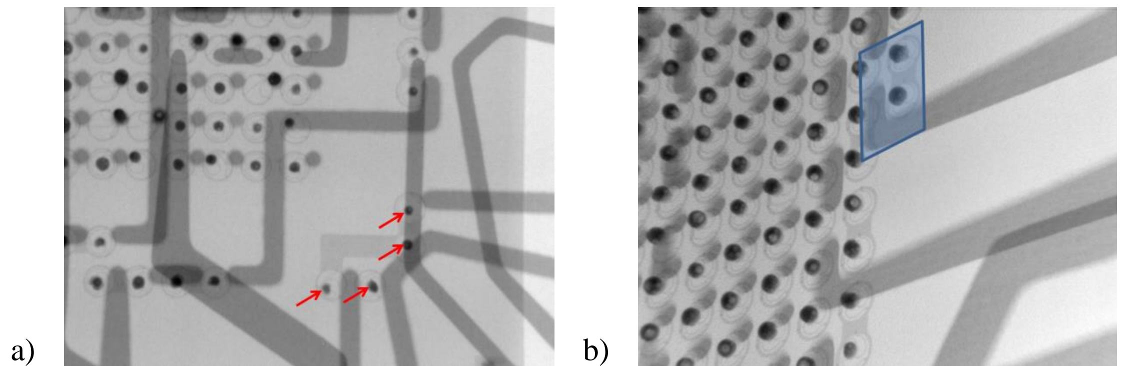


Figure 8-11: Failure resulting from interconnect to substrate pad misalignment

8.7.5. Non-parallel Assembly

Of the observed failure types listed, failures resulting from the non-coplanarity of the assembled die and substrate was one of the more difficult to detect failure types. As shown in Figure 8-12, the vacuum chuck is not coplanar with the surface of the substrate. Upon placing the die and the application of compression forces, the die attempts to align with the substrate surface, but the entire compression is situated on the leading edge of the chuck, which in turn creates high compressive loads on the leading edge of die. Depending on the severity, this can result in a complete open of the back edge of the die as shown in Figure 8-13b.

A top down view inspection of the sample does not readily show a problem with the assembly as shown in Figure 8-13a. The image shows a well aligned sample that visually suggests a good assembly. But an inclined view of the sample shows a separation between the solder bumps and the die pads.

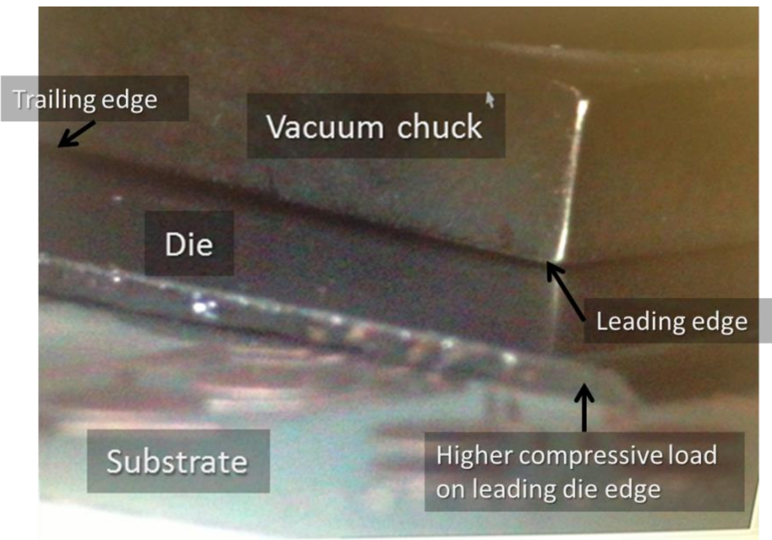


Figure 8-12: Non-parallel vacuum chucks can lead to uneven pressure distribution on assembly

The cause of this misalignment is mostly the result of gimbling the vacuum chuck on a sample which either had foreign matter or debris between the die and substrate, or the presence of a grossly over-plated solder bump as shown in Figure 8-8. The gimbling of the chuck is performed by aligning and placing the die over the substrate. The vacuum holding the die is then turned off releasing the locking mechanism that allows the chuck head to swivel. Compression force is then applied which allows the chuck to planarize itself with the backside of the die. The vacuum is then turned back on to lock the chuck in place.

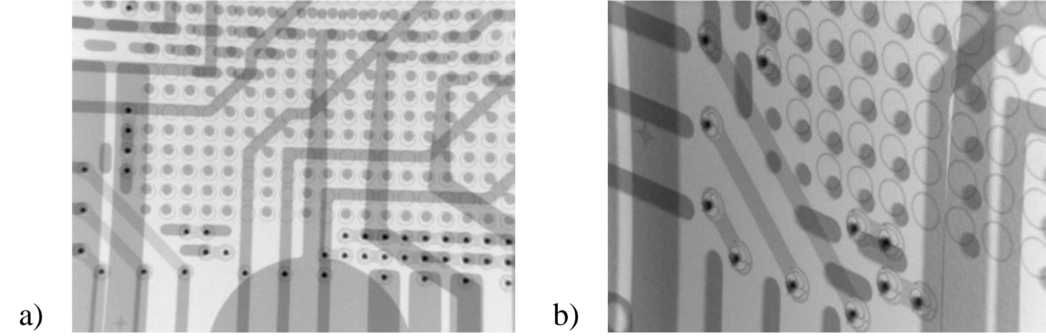


Figure 8-13: Post assembly observation of inclined die relative to substrate

Once this is done, the assembly can then be performed. During thermo-compression bonding, the vacuum chuck holds maintains its orientation through reflow of

the solder. In a case where the solder heights are not uniform, this can help correct such problems provided that the chuck is coplanar with the substrate. Otherwise, the chuck could very well be responsible for creating the failure. Following this discovery, subsequent assemblies used bare silicon pieces to planarize the chuck with respect to the surface of the substrate.

8.7.6. Non-reflow of Solder

Non-reflow of the plated solder was amongst the more unpredictable of the observed failure patterns. Some reasons for the failure to reflow of plated solder include excessive oxidation of the solder, not enough flux around the solder or an excess amount of silver in the alloy. With a heavily oxidized solder sample, reflow studies conducted under an optical microscope reveal that the core of the solder reflows at the eutectic temperature. In a lot of cases, the melt pool is unable to dissolve the outer oxide layer which is necessary in order to form a bond with neighboring objects.

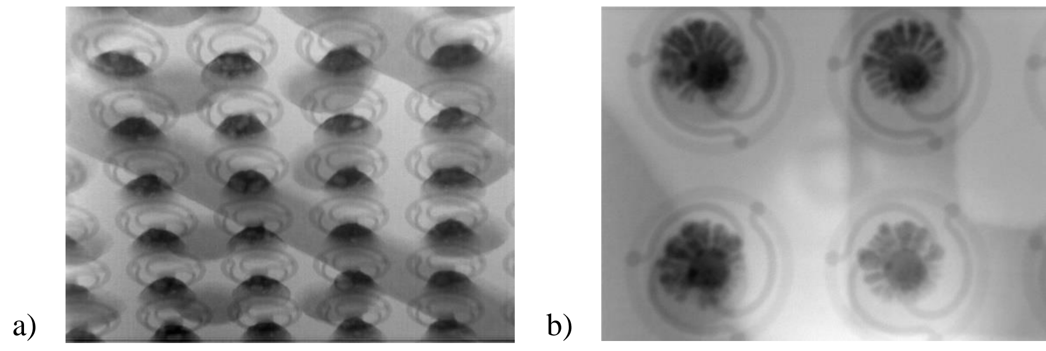


Figure 8-14: Comparison of a) reflowed solder in an assembly to b) a failed reflow also in an assembly

In the case of a deficiency of flux around the solder, the elevated temperatures build up thick oxide layers on the solder leading to the first condition. The third condition is caused by conditions during the electroplating deposition of the solder. The composition of the deposit during plating is strongly dependent on the ratio of silver in the tin bath. Excess silver in the bath equates to an excess of silver in the deposit, which

according to the phase diagrams of tin-silver can lead to higher than expected reflow temperatures of such an alloy.

Figure 8-14 compares a successfully reflowed sample with one in which the solder failed to reflow. In the reflowed sample, the solder from the interconnect flares out from the copper pad to surround the larger substrate pads beneath. With the unreflowed solder, this profile was not observed. However, Figure 8-14b shows distinct features usually observed on the plated solder samples such as those shown in Figure 7-18.

Corrective measures taken with this failure type was to ensure that the plating baths constituents were within recommended the ranges, and also the plating current densities. Lastly, sufficient amounts of flux were applied to samples to ensure complete coverage of the solder. Excess flux not consumed during assembly can be removed by isopropanol after assembly is complete.

8.8. ASSEMBLED INTERCONNECTS

It is clear that the assembly process had several challenges, and assembly process development of compliant interconnects can be an exhaustive study, on its own. Following sections present results from successful assemblies which are then used for testing.

8.8.1. Assembly Yield

Following successful assembly, samples were tested for electrical continuity in the daisy chain loops and the four wire test structures. Samples which passed the continuity tests were then selected for further testing pertaining to the electrical characteristics of the interconnects or for thermal cycling depending on the substrate type on which the die was assembly. Figure 8-15 illustrates the normal deformation of the interconnects after assembly and cool down to room temperature. The deformed profile matches predictions from finite element models which also highlight regions of high stress or plastic strains after assembly. To reduce effect of damage incurred during this

step, annealing of assembled samples can help erase some of the history depending on the selected annealing temperature. Recommended temperature ranges are between 100 ^{o}C to 150 ^{o}C. Lower annealing temperatures create a lower stress free temperature for the interconnects, thereby reducing accumulated damage.

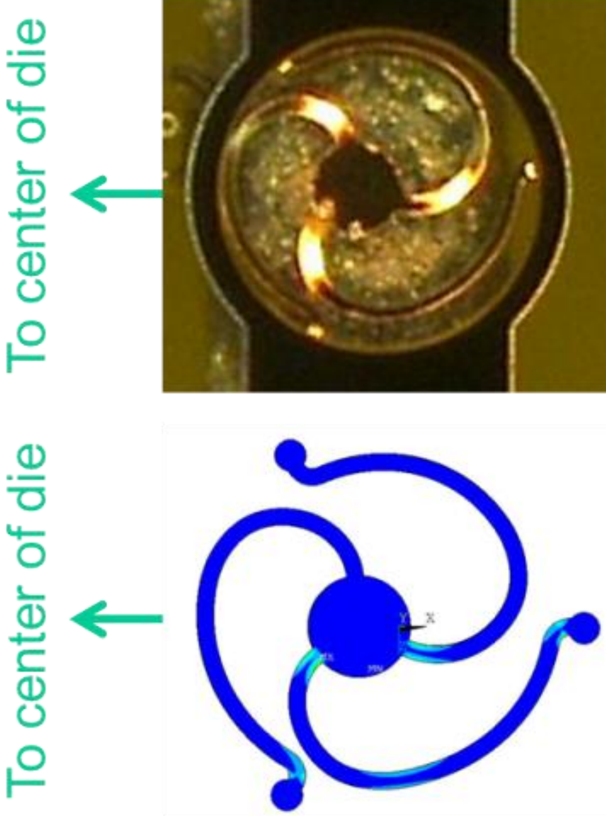


Figure 8-15: Assembled interconnect

CHAPTER 9

EXPERIMENTAL CHARACTERIZATION AND RELIABILITY ASSESSMENT

9.1. INTRODUCTION

Physical characterization of experimental prototypes is an important aspect of the interconnect development. In addition to mathematical models and simulated predictions, it is important to ensure that the physical prototypes perform as well as the simulated predictions. For this reason, assembled and unassembled fabricated samples were subjected to several tests to compare their physical responses to those predicted by models. In this chapter, the results from electrical and mechanical tests are presented and discussed.

9.2. ELECTRICAL TESTS

The electrical tests carried out on the fabricated interconnects were non-destructive in nature. The tests of interest were tests related to the performance of these interconnects for signaling applications, which include resistance measurements and the measurement of the scattering parameters.

9.2.1. Resistance

Electrical resistance measurement is perhaps the best indicator of the performance of current carrying devices. The physical determination of electrical resistance is straight forward and does not require elaborate equipment and software to interpret the measured data. To determine the resistance of the fabricated interconnects, samples were subjected to four wire measurements to exclude the effects of contact resistance and the resistance of the test leads from the measured data. In order to carry out direct resistance measurements, two approaches were taken. The first approach involved direct inquisition of the interconnects using probing tips, while the second was conducted via the four-point Kelvin structures in-built into the substrate design.

9.2.1.1. Direct Probing

Direct probing of the interconnects was useful and necessary, as it enabled probing of interconnects that were not located along the outermost edges of the die where the Kelvin structures were located.

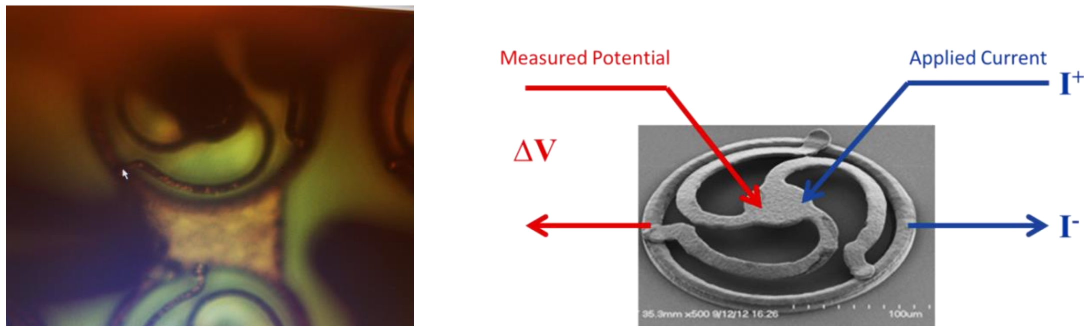


Figure 9-1: Four point measurement setup using probe station

To enable direct inquisition of these micro-structures, a Signatone® probing station hooked up to a Keithley® source meter and a Keithley® multimeter were used. The probe station's stage and probe holders were equipped with micrometer dials to enable precision movement. Illustrated in left image of Figure 9-1 is one such interconnect during setup as viewed through the probe station's microscope. The darker features in the bottom corners of the image are two of the probe tips and the other two tips are located at the top of the screen close to the center pad of the interconnect. Owing to the relative sizes of the probe tips compared with the interconnects, connecting the two probe tips proved somewhat challenging. In order to establish a good electrical connection with the center pad, the first probe was brought close to the center pad and then advanced slowly until it just touched the pad so as not to deform the interconnect. The second tip was then brought in from the opposite direction until it made contact with the pad. The probe was then used to push the pad against the first probe until stable contact was achieved. Placing the bottom probes posed no challenges as the rings (annular copper pads) to which they were connected was firmly anchored to the base substrate.

To help illustrate the setup, the right image in Figure 9-1 is a schematic of the four-wire probe tip placements on the interconnects and their functions. Using the Keithley source meter, 5 mA of current was sent through the probing tips designated by *I*. The flow of current through a lossy conductor such as copper creates a potential drop across the interconnect. With the second pair of probing tips, the potential drop across the interconnect was then measured from which the resistance of the interconnects were calculated using Ohm's law. The measured resistance of the interconnect was found to be 15 mΩ. A finite-element model with the same dimensions, as the fabricated interconnect, was then created. Using the resistivity value of pure copper, the model yielded a resistance of 14.2 mΩ. The difference between these numbers could be attributed to the resistivity value of copper used in the models.

9.2.1.2. Resistance of Assembled Interconnects

Kelvin Structures built into the substrate design enabled hassle-free probing of the four wire resistance of the interconnects. To enable four wire measurements of a single interconnect, 3 to 4 interconnects were used in total to send and receive current and measure the potential across the target interconnect. Figure 9-2 illustrates the layout of the test structures. Current was passed through one path of the substrate traces and up through an interconnect and into the die trace from which it returns through the target interconnect and then back through the receiving trace.

The potential across the target interconnect was then measured by probing the traces connected across the target interconnect. The first voltage measurement path travels along one trace and then up through the interconnect, then goes through the target interconnect via the die trace and back through its return path. To ensure accuracy of the measured results, it was important to ensure that the only portions where the current and voltage paths overlapped were only in the target interconnect. Otherwise, the resistance

of any overlapped regions would be included in the measured resistance, skewing the results.

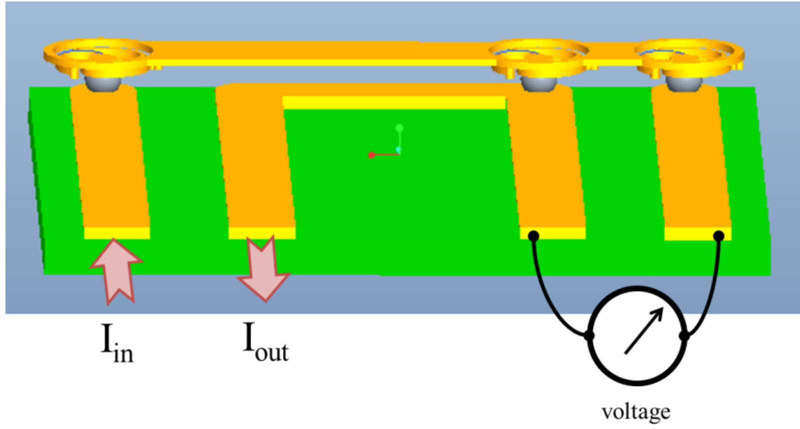


Figure 9-2: CAD illustration of inbuilt four wire measurement structures in test vehicle

With the four wire test structures situated at the periphery of the test vehicle, they were only capable of measuring the resistance of the primary interconnect structures. The average measured value of the resistance of the high compliance interconnect based on several samples is about 19 mΩ. This is about 30% higher than the measured resistance based on direct probing. This difference can be attributed to the presence of the solder bonding the interconnect to the substrate in the assembled configuration. The samples directly probed for electrical resistance did not have plated solder as illustrated in Figure 9-1.

The solder used in this fabrication was eutectic tin-silver solder which is composed primarily of tin. With an electrical resistivity at least four (4) times that of copper, the solder resistance is also included in the measured resistance. For simplicity, the solder in the assembly can be assumed to be a 40 µm tall cylinder with 40 µm diameter. Based on a resistivity of value of 7.78e-8 Ωm, the resistance introduced by solder will be 2.5 mΩ accounting for over 60% of the observed difference in resistance between the directly probed and assembled samples. The additional resistance could be

attributed to trace fringe resistances and possibly the trapped air/flux pockets normally observed with reflowed solder.

9.2.2. High-Frequency Response

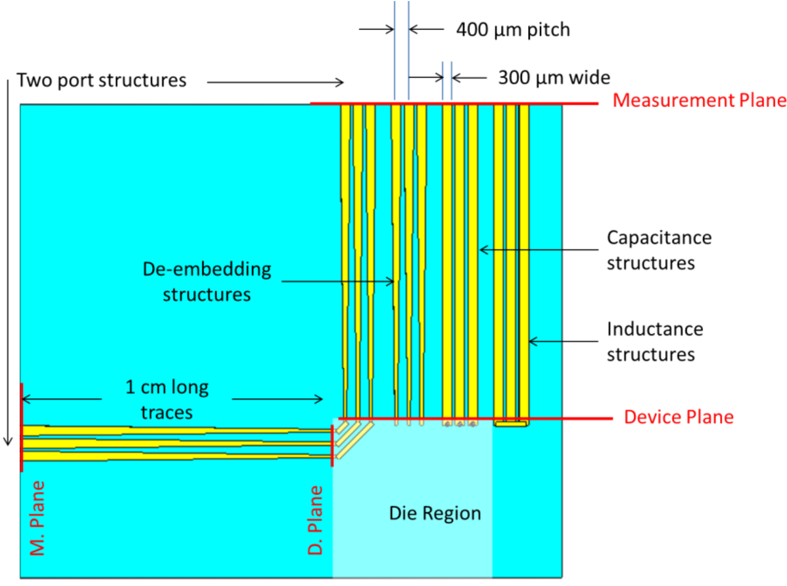


Figure 9-3: Electrical test structures for measuring the scattering parameters of the interconnects

Tools that enable direct measurement of the inductance or capacitance of the interconnects were not readily available, therefore an alternate method to quantify the impact of the parasitics of the interconnects was implemented. Insertion loss, which is perhaps the most useful electrical parameter to characterize the deterioration of transmitted signals, was used. The insertion loss of assembled interconnects was obtained through measurements of the scattering parameters of the assembly. Figure 9-3 illustrates the layout of the test vehicle used for the measurement of the scattering parameters. The two port structure with measurement planes on either side of the test vehicle was measured using an Agilent® virtual network analyzer with Cascade GSG500 probes. GSG stands for ground-signal-ground and 500 represents the pitch of the probe tips in microns. For the measured samples, the 200 µm pitch size scale interconnects were separated by a pitch of 400 µm to accommodate the probe tips. The measurement plane referring to the

point where the probes were connected to the test vehicle also had a pitch of 400 µm with the traces being 300 µm wide as illustrated in Figure 9-3.

The scattering parameter characterization structures on the test vehicle were designed by a student in the Mixed Signal Design Group at Georgia Tech. The test structures included features for single and two-port measurements and an additional feature for de-embedding the effects of the traces. For the selected test range of these structures, between 10 MHz and 20 GHz, the 1 cm long traces leading to the interconnects act as transmission lines and their effect dominates the measured data. This made it necessary to de-embed the impact of the transmission lines from the measured data in order to determine the parasitics of the interconnects alone.

The two-port test structures give the capability of determining the parasitics (R, L, C) of the interconnects using appropriate decomposition equations. Through a two-port measurement, the entire spectrum of the scattering parameters can be obtained. These include S11 and S22 parameters, which are the return losses measured at ports 1 and 2 respectively; and the S21 and S12 parameters, which are the insertion loss for a signal sent through port 1 and measured at port 2 for the S21 measurement. The corollary is true for S12. The measured insertion loss of the test samples are indicated by the red and green curves in Figure 9-4. The responses from both samples are almost identical across the test range which suggests good quality data.

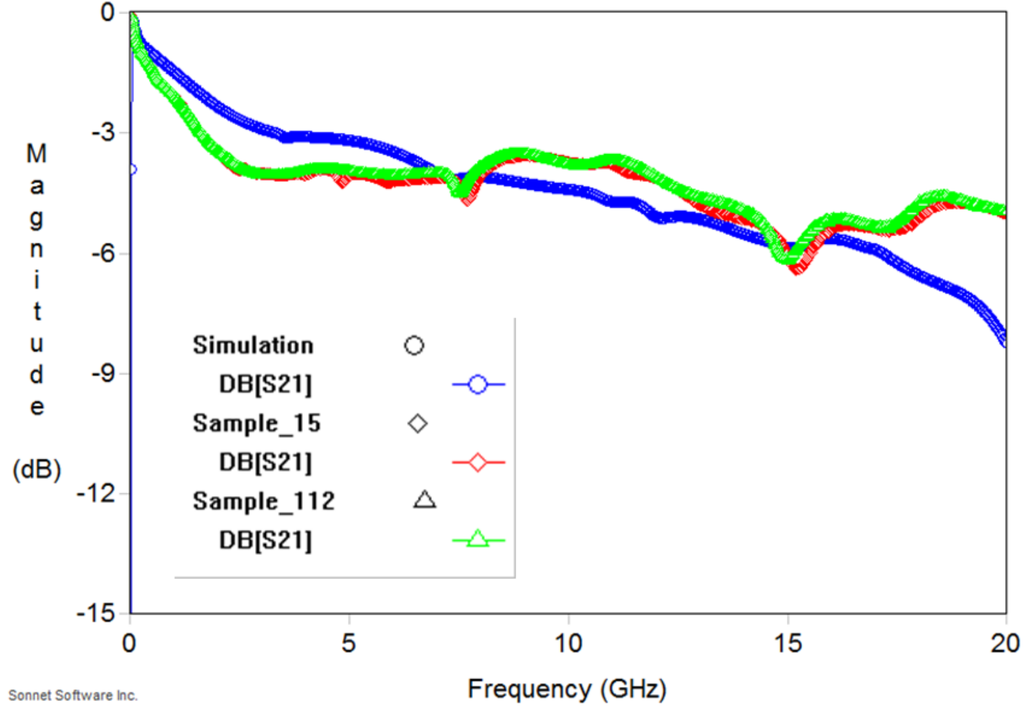


Figure 9-4: Plots comparing simulated response against measured insertion loss (S21)

Due to difficulties de-embedding the effects of the transmission lines from responses of the interconnects, a software-based approach was used to extract its scattering parameters. A CAD model representative of the test assemblies was created in Pro-Engineer®5 (Figure 9-5) and exported into CST® which is an electronic design automation (EDA) tool for electro-magnetic simulations. Using the supplied material properties from vendors, simulations were performed to recreate the insertion loss measurements from the test samples. The material properties were then calibrated to create a better match between the simulated and experimental responses as illustrated by the blue curve in Figure 9-4. Overall, the simulation does seem to correlate the measured responses implying that parasitics of the Delta interconnects can be obtained from the simulation of the interconnects model.

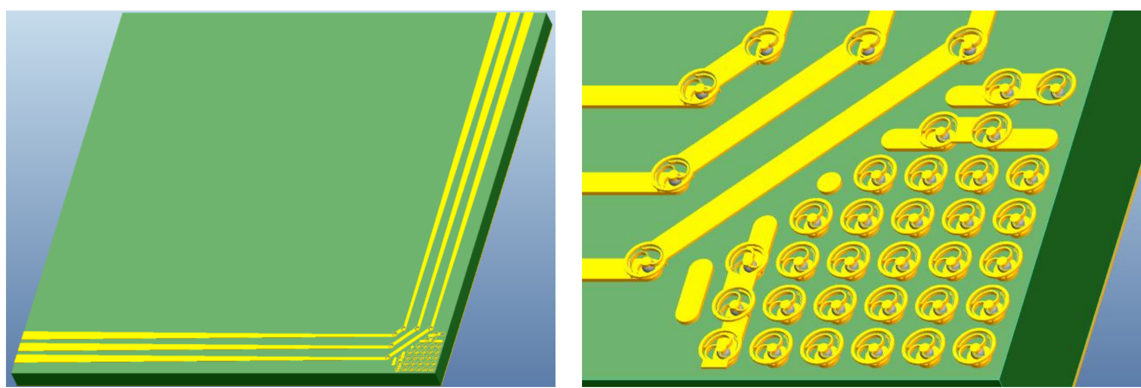


Figure 9-5: CAD model representing assembled fabricated structures characterized for electrical performance (the die is hidden in this view)

Using the adjusted properties, a model of a pair of interconnects inclusive of their copper pads and solder bumps was then created. The interconnect pair was situated between a silicon die and an FR4 substrate. Figure 9-6 shows the ports setup used for the simulation.

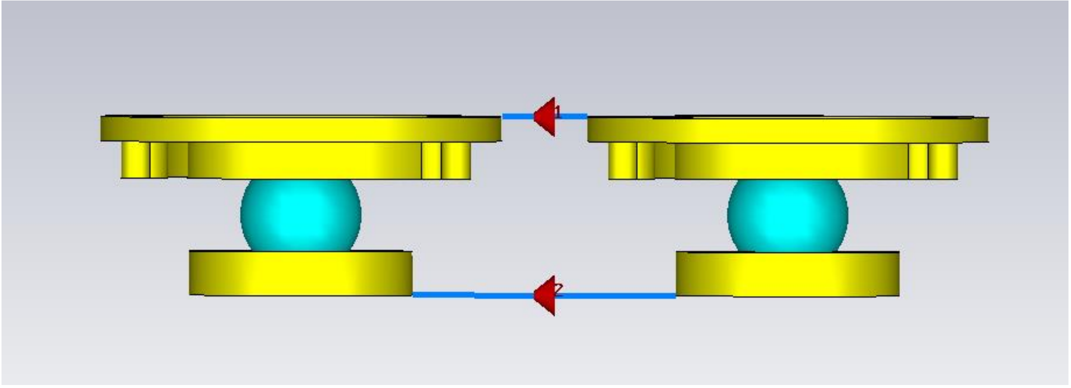


Figure 9-6: Interconnect pair with adjust properties to simulate response of interconnects alone

Figure 9-7 shows the insertion loss of just the interconnects (pink line) in comparison with simulations with the transmission lines. As can be seen, the losses associated with the interconnects are negligible and affirm that the transmission line effects dominate the measured data. From the simulation result, the attenuation of the interconnect's response at 20 GHz is only 0.273 dB. Considering that there is nearly a 250% difference between the simulated response and the measured data at 20 GHz (Figure 9-4), a more appropriate location for comparison is at 15 GHz, where both

quantities match. At 15 GHz, the attenuation of the interconnect pair is only 0.169 dB. Since the 15 GHz point gives the highest attenuation of the measured data according to Figure 9-4, the impact of the interconnects on transmitted signals at up to frequencies of 20 GHz is minimal. This suggests that Delta interconnects are well suited for high frequency applications.

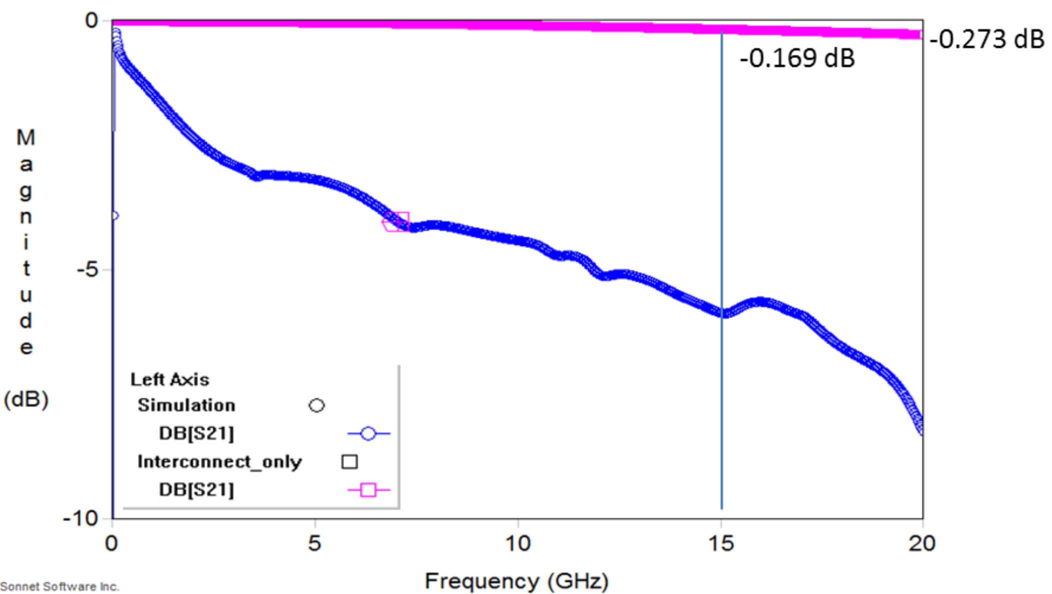


Figure 9-7: Simulated interconnect response based on full scale model material adjusted model

9.3. MECHANICAL TESTS

9.3.1. Compliance

Physical compliance measurements were performed on fabricated samples to compare predicted compliance values with actual. Out-of-plane compliance tests and in-plane compliance tests are performed and through the load-displacement graphs from these tests, the compliance values are reported.

9.3.1.1. Out-of-Plane Compliance

The out-of-plane compliance testing of the interconnects was performed using a Triboscan® nano-indenter. The test setup was identical to that used in the compliance models shown in Figure 9-8. A die sample with fabricated interconnects was fastened to nano-indenter's work table. A load tip was then used to apply a prescribed amount of force to the interconnect in the out-of-plane direction while recording its displacement. One such force displacement curve is shown in Figure 9-9. From the unloading curve of Figure 9-9, the compliance of the interconnect was calculated to be 5.00 mm/N. This is several orders of magnitude higher than comparable solder bumps of the same pitch.

Compliance simulations with the fabricated cross-sectional dimensions gave a compliance of 2.19 mm/N; a difference of about 50% compared to the measured compliance value. A possible reason for the discrepancy could be from the modulus of copper used in the model. Literature shows that the modulus of electroplated copper could vary widely depending on the plating parameters used. For example Miura et al. reported a modulus range between 30 GPa to 200 GPa for electroplated copper [25]. Repeating the out-of-plane compliance simulations for the modulus range of 30 to 200 GPa gives a compliance range of 8.76 to 1.34 mm/N for the interconnect which encompasses the observed value.

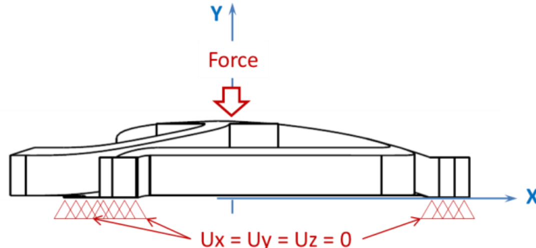


Figure 9-8: Out-of-plane compliance setup used in both physical tests and simulations

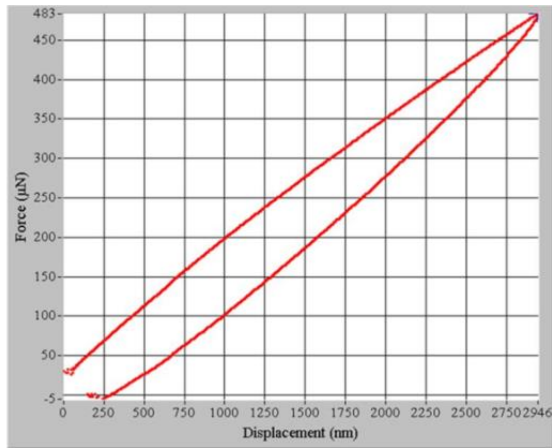


Figure 9-9: Load-displacement curve for high compliance interconnect

9.3.1.2. <u>In-plane compliance</u>

In-plane compliance of the fabricated interconnects could not be performed on the tribo-indenter as the tool was only capable of applying loads in the out-of-plane direction. Furthermore, the tool tip would need to be small enough to fit into the pockets created by the arcuate beams shown in Figure 9-10a in order to push the center pad horizontally.

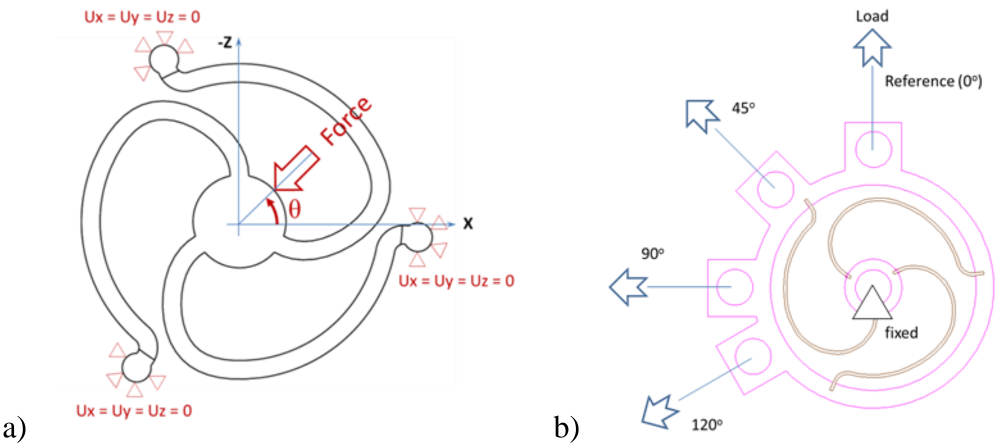


Figure 9-10: In-plane compliance setups used for a) simulations and b) physical tests

The solution adopted to determine empirically the in-plane compliance of the Delta interconnect was to create a scaled version large enough to be mounted on a tensile tester. To achieve this, the interconnects were scaled up 100x large enough to be handled without damage. The samples were created through standard photolithographic processes using photoresist deposited on a wafer sputtered with titanium as an adhesion and release

layer followed by a copper seed metal to define the pattern. The thickness or height of the fabricated sample is 100 µm and the measured widths of the arcuate beams were about 250 µm. To ensure good quality data from these samples, the geometry of the arcuate beams were altered from the designed values. Ordinarily the widths of the scaled beams would have been about 600 µm wide but with a photoresist coat of only 100 µm thick, the geometry of generated structures would have been prone to deforming in the out-of-plane direction. Therefore the widths were reduced to about the same size as the thickness of the photoresist as shown by the samples in Figure 9-11 to ensure in-plane deformation only.

The photoresist used for this fabrication was AZ40XT spun to a thickness of about 110 µm. Using the same copper plating bath as the fabricated interconnects, these samples were plated. The plating rate used was about 5 mA/cm^2 for a duration of 14 hours.

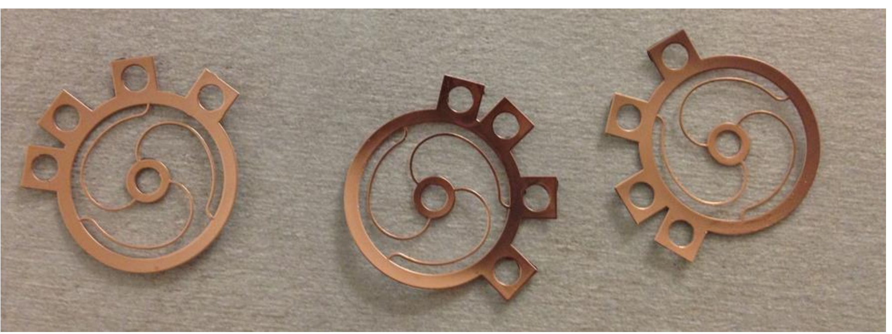


Figure 9-11: Macro-samples created to enable the measurement of in-plane compliance

Prior to testing, the released samples were first annealed between 2 copper slabs in an oven at 150 ^{o}C for about 1 hour. The process was intended to relieve the samples of the tensile stresses built-up during the plating process. After annealing, these samples were attached to a tensile tester as shown in Figure 9-12 to obtain their load-displacement responses. To enable the determination of the directional compliance of these interconnects, load handles at 0°, 45°, 90° and 120° were created as shown in Figure

9-10b. Through cyclic symmetry, the measurements from these angles can be extended all the way to 360°.

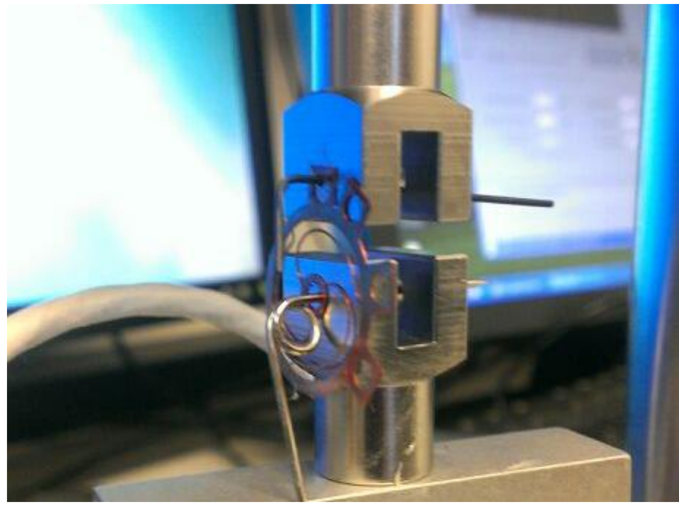


Figure 9-12: Macro-sample setup for compliance testing

The load-displacement curve from one such test is shown in Figure 9-13. The initial portion of the data show the load pins adjusting around the interconnect. This is followed by a gradual rise in force up to a displacement of about 0.5 mm. The displacement loads were kept low for two reasons: the first was so as to not exceed the elastic limit of the interconnect, and the second was to ensure that the deformation of the interconnects stayed within the plane of the applied loads. The inverse slope of the unloading curve highlighted in red was used to compute the compliance of the interconnects.

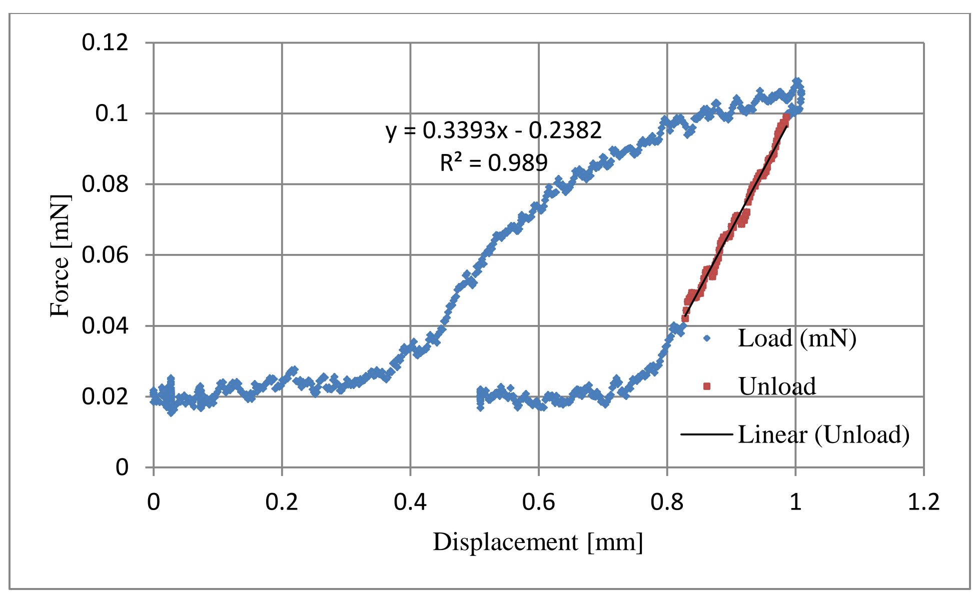


Figure 9-13: Load versus displacement response of macro-samples

Figure 9-14 is a plot of the measured compliance values as a function of load orientation. Based on this plot, the compliance of the interconnects show near uniform responses for various angles of load application. Much like the results obtained from simulations in Chapter 4, the compliance of these interconnects are insensitive to load direction. Simulations as a means to validate the in-plane compliance models were carried out for copper with modulus between 30 – 200 GPa to cover the range of expectable thin film copper modulus. The simulated compliance of the in-plane structures was between 1.2 mm/N and 8 mm/N and bounds the measured average compliance of 2.7 mm/N. Thus, it can be inferred that the simulated compliance results under Section 6.4. describe the responses of the Delta interconnects at the micro-level.

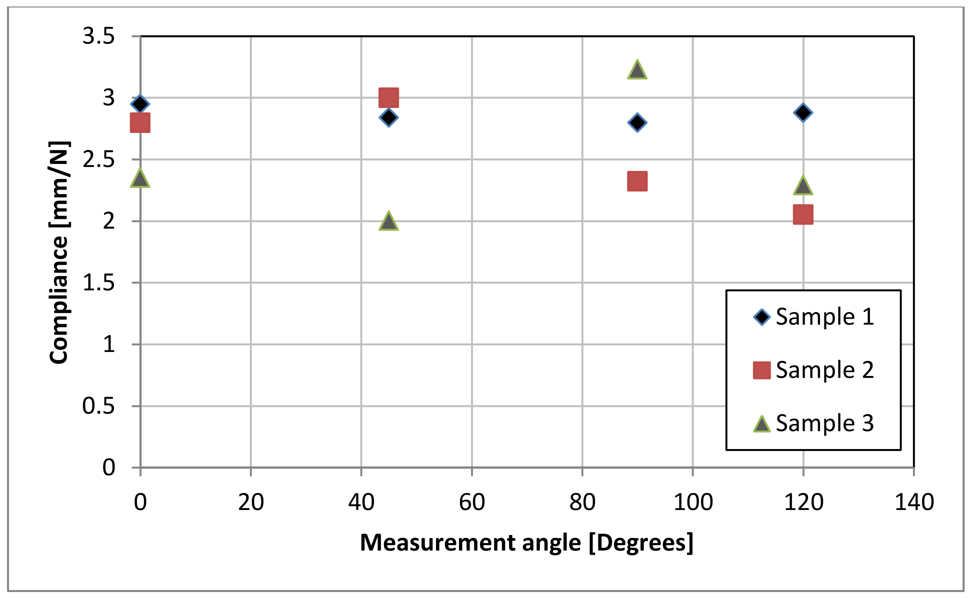


Figure 9-14: Compliance results of macro-samples as a function of load orientation

9.3.2. Structural Integrity under Shear Loads

Structural tests to check the fidelity of the bond between the interconnects and the silicon dies were carried out using a Dage ball shearer. These tests were carried out on as fabricated dies with interconnects, prior to assembly to organic substrate. These tests were intended to explore whether the interconnects can deform laterally without being sheared off from the die pad. Thus, die samples with interconnects were affixed to the work table of the tool and the stylus of the ball shearer was used to push the interconnects until they were grossly deformed as shown in Figure 9-15. Specific checks conducted were to determine the integrity of the bond between the interconnects and the annular pads and between the annular pads and the silicon die. Owing to the relative size of the structures and the high compliance of the interconnects, the sensitivity of the load head used for this test was not enough to register the low forces needed to deform the interconnects. The interconnects were tested in 3's to increase the deformation load. However, it was not enough to be detected. The results presented here are therefore qualitative in nature and show that the interconnects will not shear off from the copper

pads even under gross deformation. Deformed interconnects can be found directly in front of the tool wedge tip and immediately to its left. These tests show that the Delta interconnects have good structural integrity for the purpose to which they were designed.

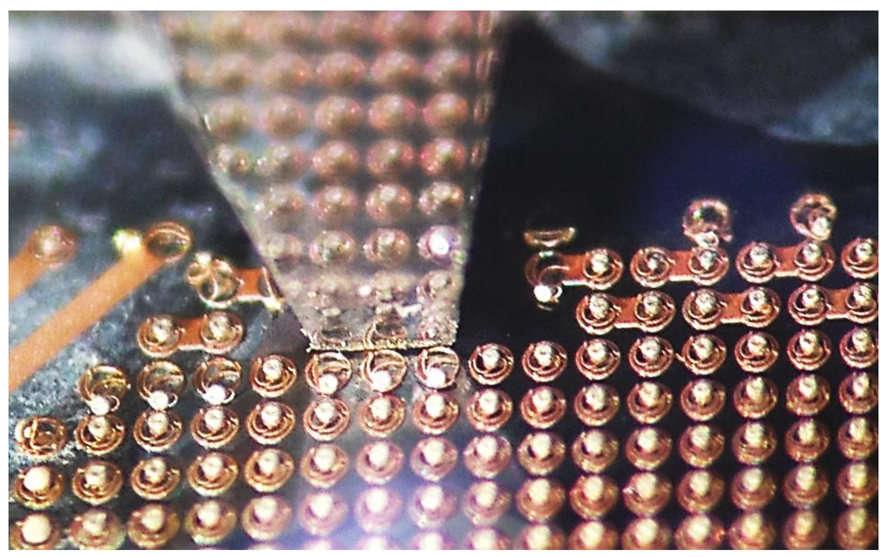


Figure 9-15: Structural integrity tests checking adhesion of fabricated interconnects to the annular copper pads and to silicon

9.3.3. Assembly Warpage

Following assembly, samples were tested for electrical continuity in the daisy chain loops and the four wire test structures as check for assembly. To observe the impact of the stiffness of Delta interconnects on the warpage of assembled dies, one of such assemblies was placed in a contact profilometer and the back side of the die scanned for changes in elevation. The stylus of the profilometer was situated along the mid-line of the die and run across the entire length of the die. To avoid damage to the stylus tip or the profilometer, only 19.5 mm of the possible 20 mm length of the die was scanned. Figure 9-16 shows the profilometer reading of the die's back side elevation with respect to its spatial location. This plot shows that at room temperature the assembled sample has minimal warpage.

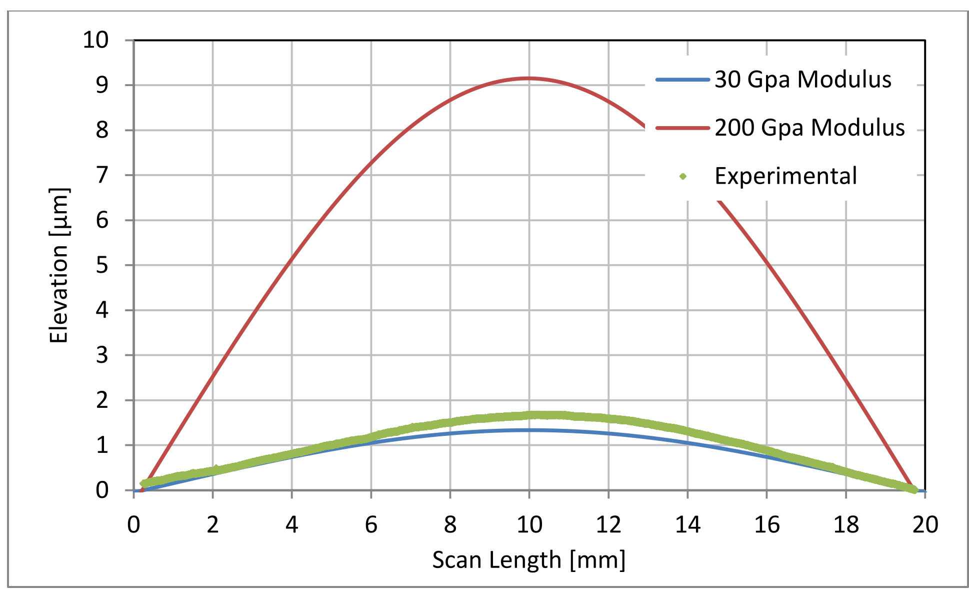


Figure 9-16: Measured assembled die curvature at room temperature compared with simulation

To accommodate the variations in the range of observed thin film copper properties, warpage simulations using the upper (200 GPa) and lower bounds (30 GPa) of the modulus of copper were performed. The warpage of the physical die is seen to fall within these limits. From the data, it can be deduced that the modulus of the deposited copper is close 30 GPa. The experiments and simulations show that the interconnects can mechanically decouple the die from the substrate, and thus, can reduce the warpage of the assembly. As discussed earlier in Section 6.4.2. , the interconnects will be able to reduce the warpage as well as the induced stresses in the die by the mechanical decoupling.

9.3.4. Thermal Conditioning of Fabricated Samples

Electroplated copper films tend to have residual stresses built-up during the plating process. The deposition process tends to create tensile stresses in the deposited copper films. For thin deposits, this stresses are usually low and unnoticeable, but at higher plating rate and for thicker deposits, these stress values cannot be ignored. Figure 9-17 shows two copper plated samples at different thicknesses.

The test samples shown in Figure 9-17a were fabricated on 4” silicon wafers. The process began with the deposition of a release layer. A negative tone photoresist was used as the release layer in this fabrication. Futurrex NR71-3000P was spun at 3000 rpm for 40 seconds to create a uniform resist film about 3 microns thick. The resist film was then baked at 150 ^{o}C for about 5 min to stabilize the resist. Photoresist was used as the release layer of choice to speed up the release process owing to the physical size of the test coupon handles. The handles were 2 mm wide x 5 mm long, which would otherwise require an extensive amount of release time if photoresist were not used.

A seed layer of titanium and copper (titanium for adhesion and copper as seed layer) was then sputtered over the resist to create conduction paths through which the test pieces would be plated. A second masking step was used to create the micro-molds for the test specimen. A positive tone resist supplied by Shipley (Megaposit SPR 220) was used for the second resist step. SPR220-7 was spun at 800 rpm for about 30 seconds for a film thickness of approximately 20 µm. The resist was then baked at 100 ^{o}C for about 5 min on hotplate. The resist was then patterned using a contact aligner to photolithographically imprint the test patterns onto the photoresist. This step was followed by development in MF319 also supplied by Shipley.

The developed samples were then electroplated in a copper sulfate bath to fill in the micro-molds defined by the photoresist patterning step. Four different current densities were investigated: 3, 5, 10 and 15 mA/cm^2. For a sample with a total feature area of 23.4 cm^2, currents of 70, 117, 234 and 351 mA were passed through the seed layer to plate up the features. At the lower current densities, the samples did not peel. However, at the higher current densities, it was observed that after a few minutes of plating, the electrodeposited features would peel off from the constraining substrate into a curl. This phenomenon was observed to increase in severity with higher plating current densities. Figure 9-17a shows a sample exhibiting the observed effect. Qualitatively, it can be said that the intrinsic stresses in the electro-deposited copper increases with

plating rate/current density. To keep the samples from tearing apart, thicker seed layers were used for the 10 and 15 mA/cm^2 samples.

a) b)

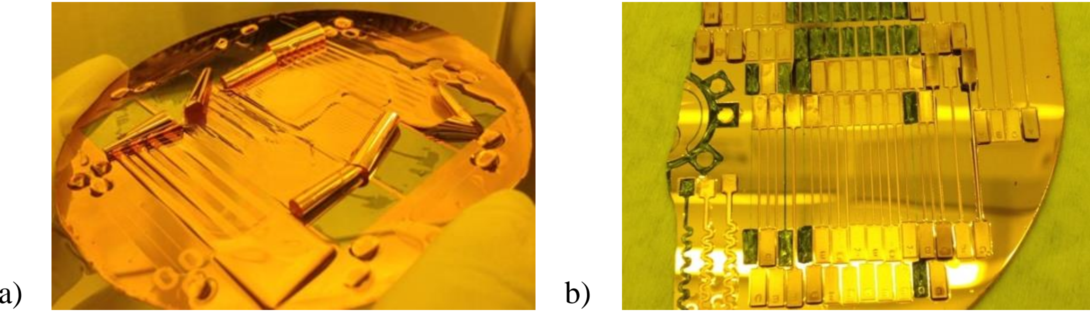


Figure 9-17: Plated test coupons @) 20 µm thick coupons on photoresist release layer b) 100 µm thick coupons on 500 nm thick titanium release layer

To create 100 µm thick samples for the out-of-plane compliance tests, based on the observations of the previous, the photoresist based release layer was substituted with a relatively thick titanium adhesion layer which doubled as a release layer. The current density was also kept low at 5 mA/cm^2 to reduce the likelihood of the build-up of excessive stresses within the films. However, owing to the much greater thickness of the plated film in the second fabrication, the effect of stress build-up seemed additive. Figure 9-17b shows test coupons from the plated sample shearing through carrier silicon and breaking out into curls. The dark spots on the sample are regions where the sample cohesively fractured the underlying silicon to relief the intrinsic stresses accumulated during electroplating. From this data, it shows that titanium is a good adhesion layer for copper on silicon/silicon dioxide based substrates.

In addition to the observed effect, electroplated copper samples exhibit low plastic deformation prior to failure in tensile tests. While they have higher strengths than annealed samples, the additional plasticity of annealed samples is preferred over strength. Based on the compliance of these interconnects and their relative size compared with the die and substrate being assembled, the displacement load subjected to the interconnect is the same for all cases, as was shown through parametric studies. In such a case, an

interconnect made of a high strength low ductility material will fail prematurely compared to a low strength high ductility version.

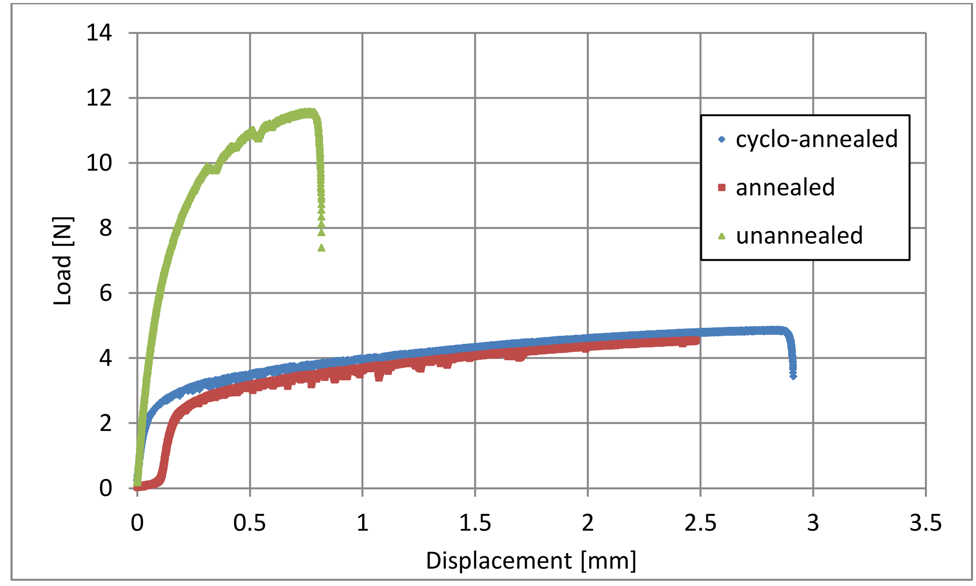


Figure 9-18: Comparison of thermal treatments on material response of test coupon

For this reason, the question of annealing the samples prior to thermal cycling came up. Will an annealed sample fair better than an unannealed sample in thermo-mechanical fatigue tests? To answer this question, test coupons measuring 20 mm in length, 250 µm in width and 10 µm thick were selected and treated to different thermal conditions. The first set was left unannealed, the second annealed at 150 ^{o}C for 2 hours in an oven, and a third set was thermal cycled between -40 to 125 ^{o}C for a duration of 24 cycles each lasting 1 hour.

Figure 9-18 is the load-displacement curves of the tested samples. The graph shows that normal annealing at 150 ^{o}C for 2 hours has the same impact as thermal cycling over a few cycles. The annealed samples (static and dynamic temperatures) show a considerable increase in ductility compared with the as-plated copper test coupon. The annealing process substitutes strength for ductility which is required to ensure that the interconnects attain reliability targets. Based on this study, annealing the fabricated samples prior to thermal cycling is unnecessary as the temperature soaks at the high limit

have the same annealing effect. However, to avoid infant mortality failures resulting from fracture of unannealed components, thermal cycling should be started at the higher temperature limit.

9.4. RELIABILITY ASSESSMENT

9.4.1. Thermal Cycling Tests

The thermo-mechanical reliability assessment of die assemblies employing the compliant Delta interconnects were performed as per JEDEC A102 standards in a thermal cycling chamber between temperatures of 0 – 100 ^{o}C. The thermal cycle chamber used was manufactured by ESPEC® and allowed programming of the temperature cycles for the intended test duration. Displayed in Figure 9-19 is the temperature profile used. The thermal cycling chamber is capable of 18 ^{o}C/min ramp rates for both heating and cooling. However, to ensure that the test samples attained the target dwell temperatures, the ramp rate used for the tests was 15 ^{o}C/min. This translated roughly to 7 min ramps and 5 min dwells at the target temperatures for a total of 24 min per cycle or 2.5 cycles per hour. As per JEDEC A102, 2.5 cycles per hour falls within the recommended 1 – 3 cycles per hour as specified for condition J.

The high thermal cycle rate is acceptable for the compliant interconnect assemblies because very little damage accrues in the solder. The Delta interconnects are at least two orders of magnitude more compliant than solder bump and in the process subject the solder to very little deformation loads. This observation is supported by simulations which show the Delta interconnects to be insensitive to thermal shock cycles.

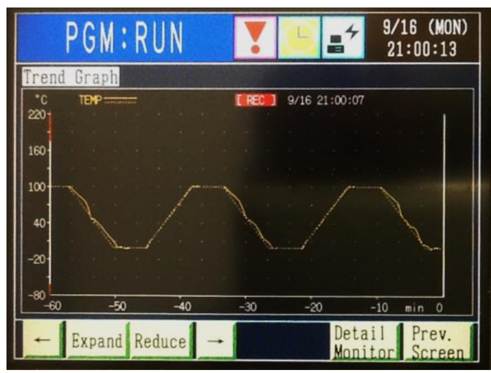


Figure 9-19: Thermal load profile used in thermal cycling of assembled samples

In preparation for testing, the test samples were placed within the tool's chamber in the path of the air stream to ensure that the samples were always at equilibrium with the air temperature. One of the test samples was wired up to a data logger for remote observation of the daisy chain resistances with time. The signal cables ran through a port in the chamber wall and terminated in a Keithley 7700 switching module. The switching module was housed in a Keithley 2700 multi-meter unit through which data logging was enabled.

To allow data storage capabilities past the 55,000 data points the Keithley buffers can hold, a remote controller was connected to the multi-meter. The controller unit through a Keithley provided software interface allowed remote monitoring of the multi-meter unit and also enhanced data storage capabilities.

Figure 9-20: Test specimens within thermal cycle chamber

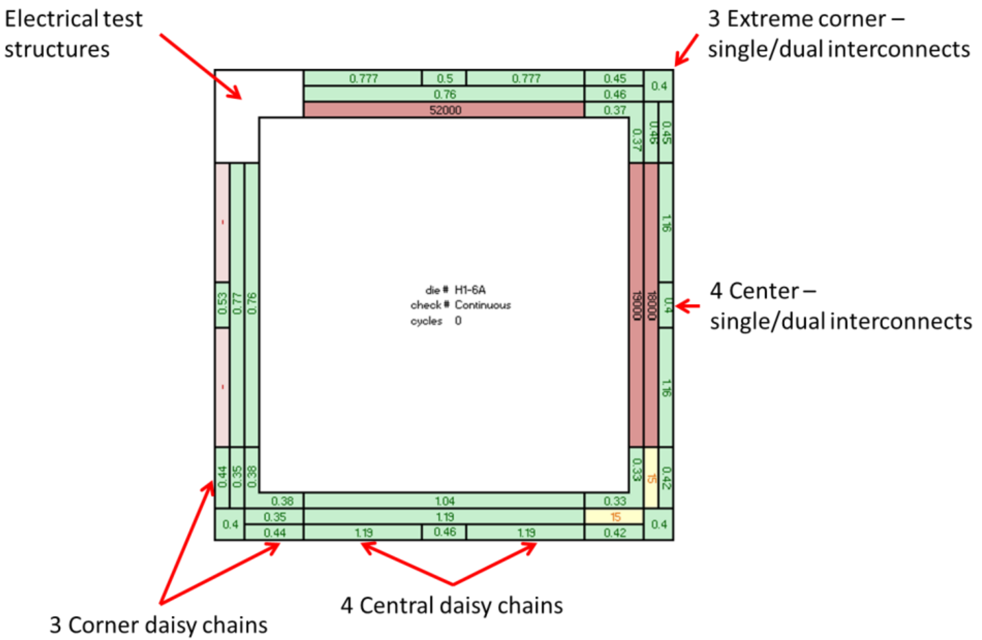


Figure 9-21: Status of daisy chains for monitored sample prior to thermal cycling

By design, the test vehicle had a total of 28 probing points to assess the status of the interconnects. Some of these test points connected only a pair of interconnects and in the case of a four wire measurement, only a single interconnect. Other test points however, connected much longer chains. The daisy chain patterns were distributed in strategic locations to observe the impact of location on the fatigue life of these interconnects. Figure 9-21 shows a distribution map of the status of the daisy chains of the sample prior to thermal cycling. Most of the daisy chains in this assembly were active except for a few damaged links. The light green links represent functional daisy chains within normal parameters. The dark pink colored links are links with unacceptably high resistance and could have been caused by an undersized solder bump making partial contact with the test vehicle. The yellow chain's resistance is higher than normal expected values but not considered failed. Lastly, the pink chain represents a daisy chain with infinite resistance typical of a damaged interconnect in the chain.

Figure 9-22 is a time based graph of the change in resistance of the monitored chains indicated by the insert in Figure 9-22. This plot shows the interconnects going up to about 840 thermal cycles before failure. The failure criteria used to determine failure was based on a 100% increase in the resistance of the observed loop.

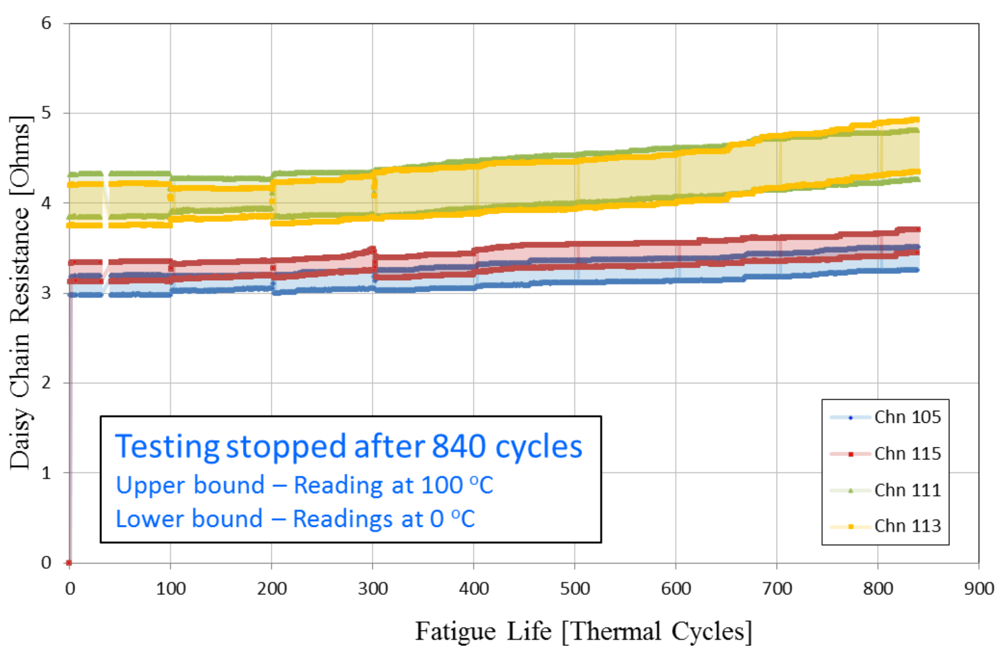


Figure 9-22: Resistance of corner interconnects over several thermal cycles

Upon the completion of the 840th cycle, the test was paused to measure the loop resistance of the daisy chain loops not connected to the data acquisition system. In particular, only the outermost corner and middle-die-edge loops were measured to determine their status. The relevance of this check was to determine if the middle-die-edge loops were still functional since they most accurately represent the strips that were modeled in finite element simulations. From the die check, 50% of the mid-die interconnects were still functional at their pre-thermal cycle resistance values.

From the overall observed failure pattern, the corner interconnects have a higher probability of failure before interconnects in other regions as predicted by finite element models. This is as a result of the larger separation between the corner interconnect and the neutral point of the die. By distribution (Figure 9-23), most of the interconnects

(including unmonitored daisy chains) survived into the 800-900 cycle range after which testing was stopped. Failures prior to 500 cycles were considered premature failures and their cause is most likely related to fabrication defects, some of which were mentioned in Chapter 8.

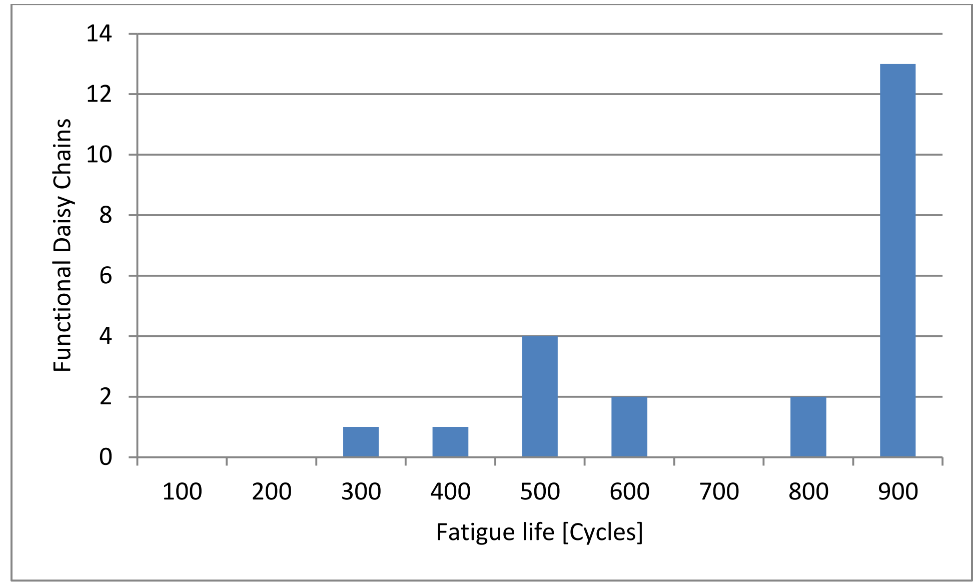


Figure 9-23: Failure distribution of interconnects

9.4.2. Thermal Shock Tests

Three other samples were assembled for fatigue life testing. To show that the fatigue life of these interconnects are ramp rate independent, they were scheduled for thermal shock cycles. Using the same conditions as with the thermal cycled sample, the temperature limits were set to 0 ^{o}C and 100 ^{o}C with 10 minute dwells at each temperature. The resulting number of cycles per hour was 3, which falls under JEDEC guidelines for condition J. As a result of the limited number of channels on the switching module used to monitor these samples, only the mid-edge interconnects were observed for these tests. The significance of this location is that it corresponds with the location on which the interconnects were designed. Hence the best performance is expected from this location.

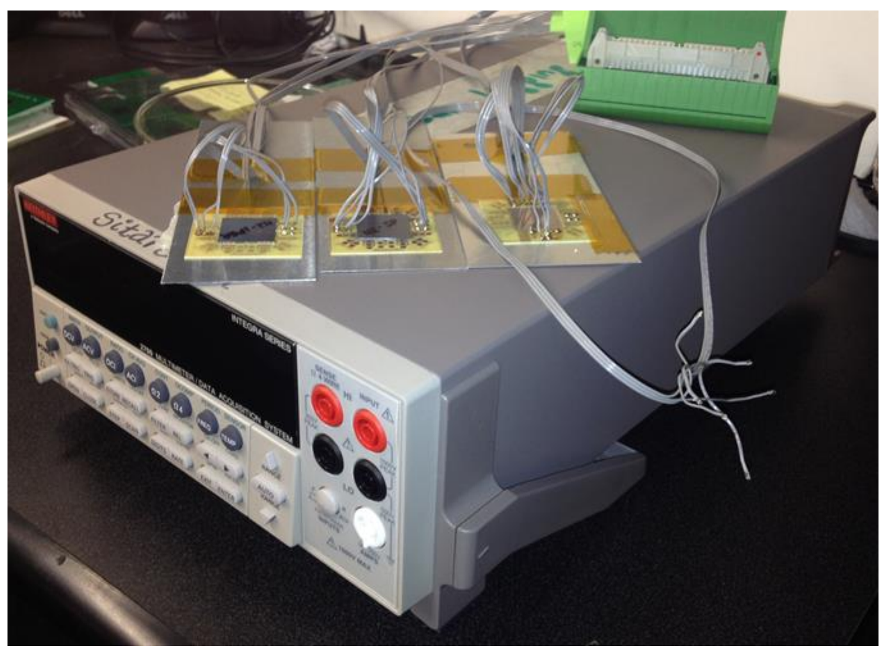
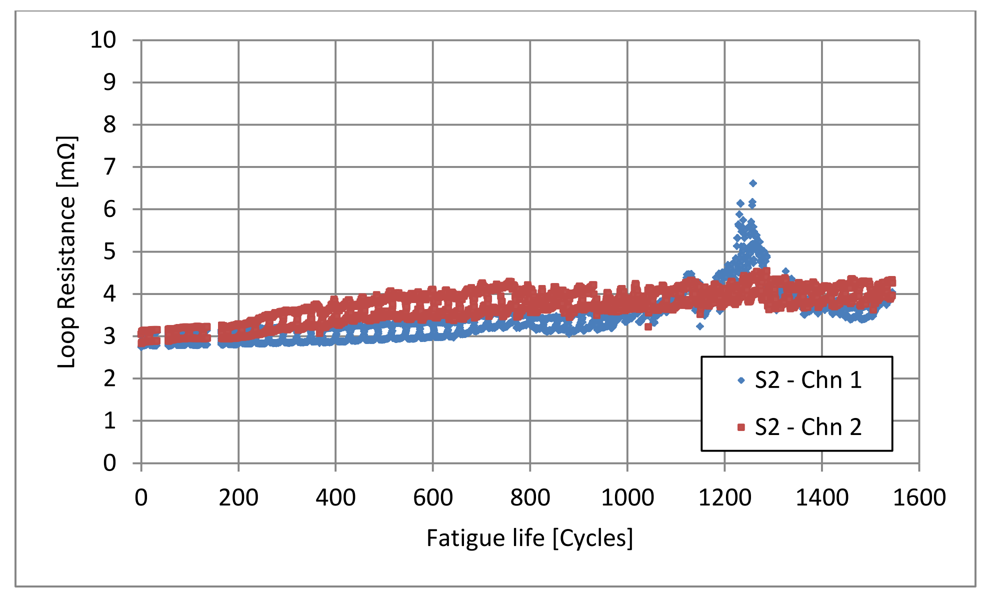
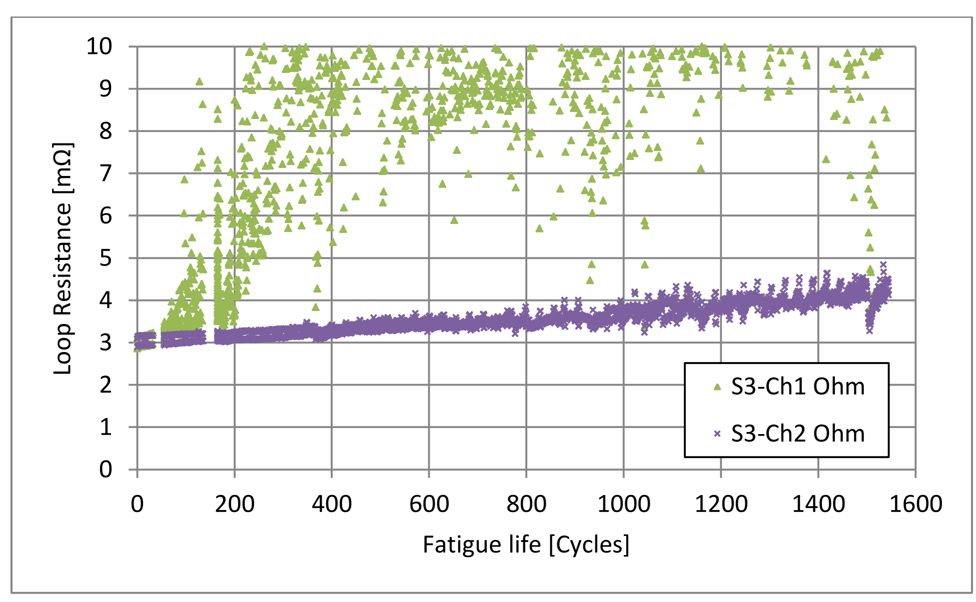


Figure 9-24: Thermal shock samples

Of the three samples subjected to thermal shock cycles, 1 sample failed prematurely at less than 500 cycles. The other two samples (samples S2 and S3) as shown in Figure 9-24 easily exceed 1000 cycles. One of the monitored chains on sample 3 shows signs of loose contact as the resistance fluctuates up and down through the test. The tests were stopped at just under 1600 cycles to allow other users access to the tool. Final resistance measurements showed these chains as functional after the completion of the tests. This shows that the compliant Delta interconnects are not only reliable, but can tolerate aggressive use conditions.



Sample 2 resistance-thermal cycle history



Sample 3 resistance-thermal cycle history

Figure 9-25: Thermal shock fatigued samples

9.5. FAILURE ANALYSIS

Due to the three-dimensional nature of the Delta interconnects, cross-sectioning of failed samples will provide little to no useful information on the failed interconnects. A different approach was adopted which utilized x-ray inspection instead. Using the Dage XD7600NT with a 750 nm feature recognition resolution, the failed samples were subjected to x-ray examinations.

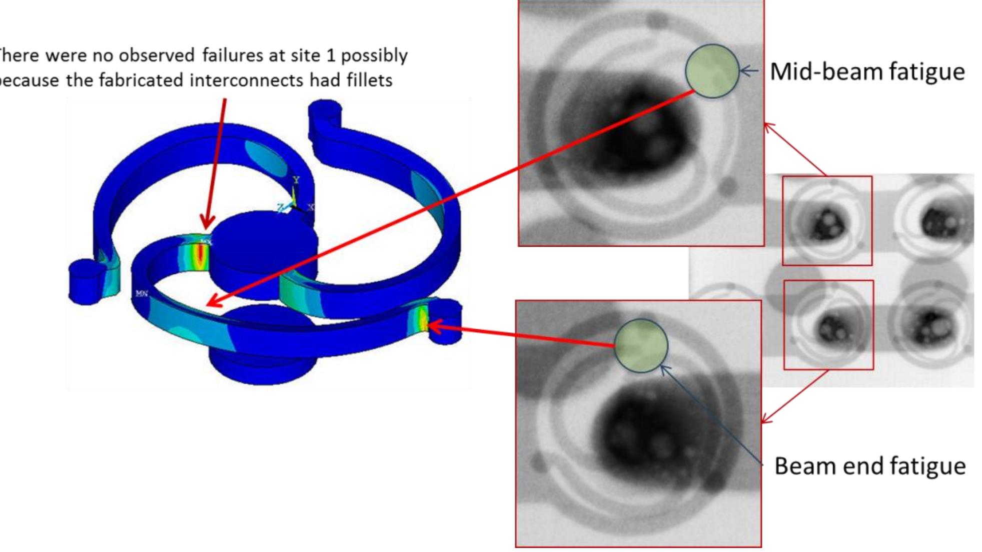


Figure 9-26: X-ray inspection of failed interconnects

Figure 9-26 shows X-ray images from one of the failed samples. X-ray inspections reveal that all failures in the interconnect assemblies occurred within the arcuate beams of the Delta interconnects as designed. This validates predictions based on finite-element models which highlight 3 potential failure sites. Failures occurred in the two regions, near the anchor and in the middle of the arcuate beam, highlighted by finite-element models as potential failure sites. By far, the dominant failure site is near the anchor or base supports of the interconnects. Based on the distribution of accumulated plastic strains in the finite element model in Figure 9-26, the preference of this site over the middle of the arcuate beam becomes clear. However, no failure was observed near the base of the center pad. This is because the fabricated arcuate beams were modified to

include fillets, and thus, the local stress concentration near the base of the center was eliminated.

Based on the experimental results, it is seen that the compliant interconnects, when fabricated and assembled through controlled processes, will be able to accommodate 1000 cycles for a 20 mm die. For smaller dies ranging from 5mm to 15 mm, the number of thermal fatigue cycles is expected to be much higher.

CHAPTER 10

HETEROGENEITY AND SCALABILITY OF DELTA INTERCONNECTS

10.1. HETEROGENEITY

Through simulations and physical tests, Delta interconnects have been shown to have desirable electrical and mechanical properties. Nevertheless, its electrical resistance is not on par with a comparable solder bump of similar pitch. One method to address this will be through the use of heterogeneous interconnects that decrease in compliance from the edge to the center of the die [15]. In a traditional die assembly such as is shown in Figure 10-1, the center of the die also known as the neutral point is a point of zero lateral displacement based on symmetry. As the die is traversed radially from its neutral point, the magnitude of the relative displacement between common points on the die and substrate increases linearly with an increase/decrease in temperature. The largest relative displacements occur at locations furthest from the neutral point. Since these interconnects are designed for relatively large dies and are able to accommodate the large displacements encountered at the edge of the die, this suggests that the inner interconnects closer to the center of the die can be replaced with interconnects with larger cross-sections since high compliance is not required in such regions.

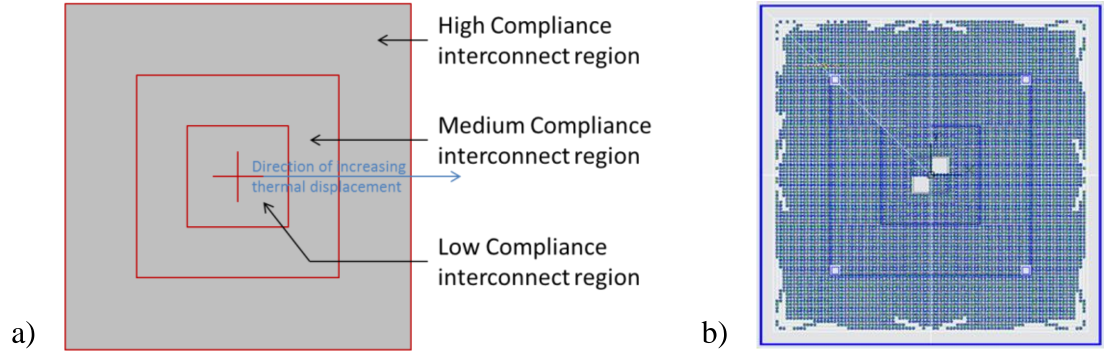


Figure 10-1: Topographical layout of heterogeneous implementation b) Mask design

In one such implementation, the die is divided into three regions, the inner, the intermediate and the outer die regions. Interconnects within the inner die are low-compliance, low-electrical parasitic interconnects, while the outer die consists of high-compliance interconnects with as designed electrical properties. The intermediate region has interconnects with properties in between those of the inner and outer die regions.

The interconnect variants created to occupy each of the three regions are listed in Table 10-1. The fabrication method for creating the heterogeneous layout uses the same procedures listed under fabrication. Since batch fabrication techniques are used, this implies that the three variants are restricted to having the same interconnect thickness. The only difference across the variants is a difference in the beam widths used. The high compliance of default design uses the nominal designed dimensions of the Delta interconnect. The intermediate's width is slightly larger by only a micron. The low compliance variant which resides in the central region of the die has the largest width. Based on its dimensions, this Delta interconnect variant can be used for power and ground I/O connection, as it can handle nearly twice as much current as the nominal design.

Table 10-1: Heterogeneous interconnects: high, intermediate and low compliance Delta interconnect variants

High Compliance	Medium Comp.	Low Compliance
Original design	Variant 1	Variant 2
6 μm width	7 μm width	10 μm width

The widths of the interconnect variants were chosen such that they were not overly

constrictive so as not to increase the intrinsic stresses in the die much above those of an assembly not employing heterogeneity. The extent of coverage of each variant was also selected such that the first failures do not occur in them. Like in the original design, failure will still occur near the die edges in the high compliance structures.

To compare the performance of such an assembly with the base design, models were created with the three interconnect variants to understand how such packages will respond in a thermal cycling scenario. The simulations used the same package size as the non-heterogeneous assembly to facilitate comparison between the two implementation types. The simulation used a strip model from a 20 x 20 mm die mounted on a 24 x 24 mm organic substrate. At 200 μm pitch, a total of 50 interconnects were modeled representing a half-symmetry strip model of a full-area array assembly.

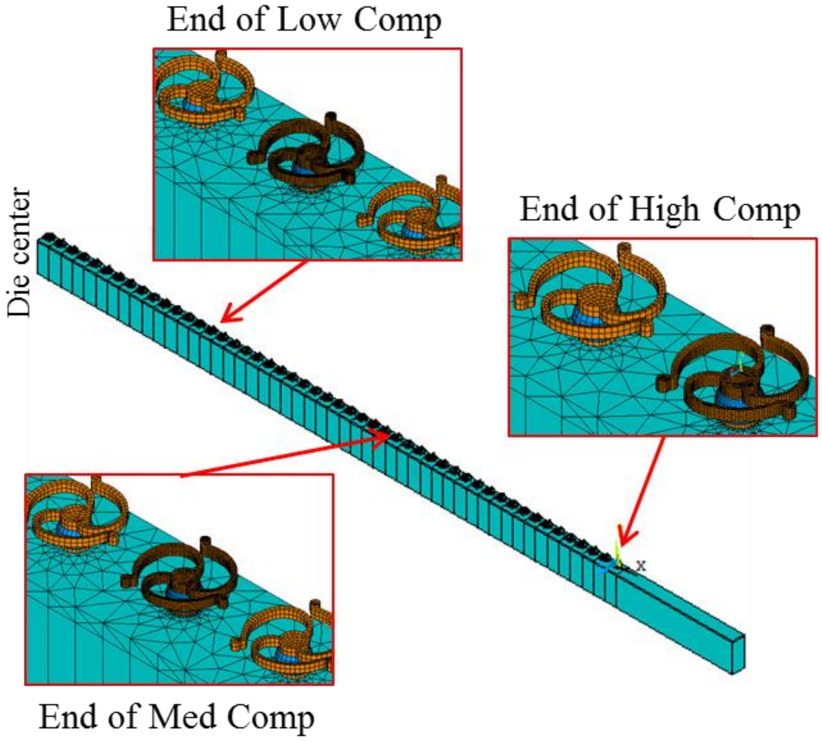


Figure 10-2: Strip model of heterogeneous interconnect layout (Die hidden)

The layout of interconnects began from the die center (left of strip). Fifteen rows of low compliance interconnects are first laid out, followed by another 15 rows of the

intermediate compliance interconnects and finally the outer 20 rows comprised the high compliance interconnects as shown. To ensure failure is captured accurately, the outermost interconnects (relative to die center) were finely meshed to fully capture the deformation strains within those interconnects. This is to ensure that failure is not overlooked within the inner interconnects and create a possibility of the first failures occurring within the inner regions of the die. All other non-critical interconnects were coarsely meshed to improve computational efficiency.

Based on the boundary conditions described in Section 5.4.1.2. , the model was constrained accordingly and a thermal load which captures assembly history as well as the first three cycles of thermal cycling between 0 to 100 ^{o}C was applied.

10.1.1. Die Stresses

Figure 10-3 shows a capture of the first principal die stresses from both the heterogeneous and non-heterogeneous (base) packages. To eliminate the influence of stress singularities as a result of undersized elements usually found around the interconnect supports, the scale bar shown in the middle has been adjusted accordingly. By comparison, the stresses induced in the base package ranges between -1.11 MPa and 3.33 MPa while the heterogeneous package has a range from -1.11 MPa to 5.56 MPa. The increase in die stresses of the heterogeneous package is as a result of substituting interconnects in the inner region of the assembly with higher stiffness variant. To put this stress in perspective, a stress of about 5 MPa is negligible in comparison with the stresses accumulated in the die during CMOS processing. For example, the resulting stresses from low temperature thermal growth of SiO_2 can get as high as 400 MPa [71].

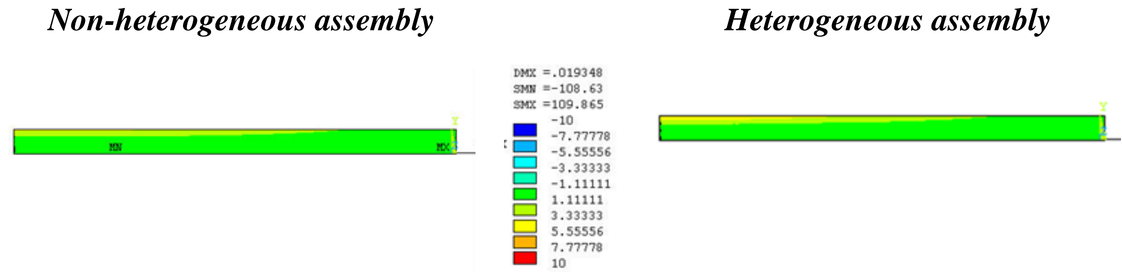


Figure 10-3: First principal stress (MPa) in die at room temperature.

Naturally, with the decreased compliance within the heterogeneous package, it is expected that the package will have a larger warpage than the base package. Figure 10-4 shows a contour plot of the out-of-plane displacements of the respective dies for the base package and the heterogeneous package. By comparison, the base package has a warpage of 5.5 μm based on a cool down of an assembled package from the reflow temperature of lead-free solder 221 ºC down to room temperature of 25 ºC. The heterogeneous package, on the other hand, has a die warpage of 7.5 μm. This represents an increase of about 36% which is only a modest increase, and considering the warpage is based on half the die length of 10 mm, this warpage is negligible.

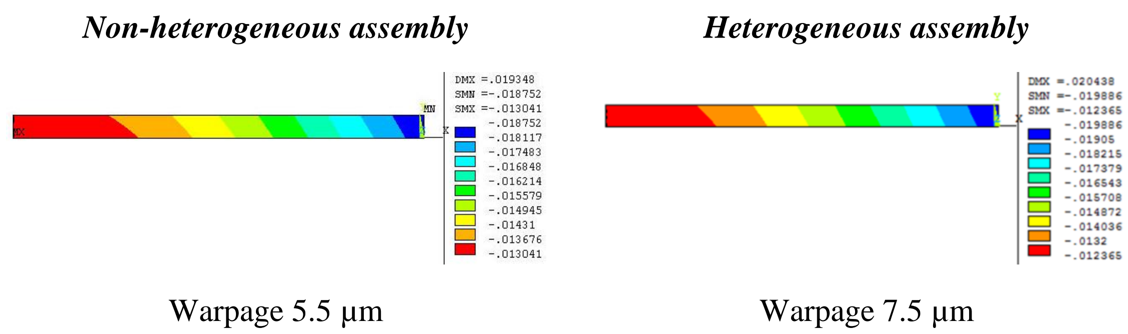


Figure 10-4: Out-of-plane die nodal displacement (mm) at room temperature.

10.1.2. Thermo-Mechanical Fatigue Life

From the package warpage, the larger warpage of the heterogeneous package indicates that the inner interconnects which were substituted with low and medium compliance variants bear more load than similarly situated interconnects in a base

package configuration. It is therefore expected that the outermost interconnect in the heterogeneous package will accumulate less damage than a similarly placed interconnect in the base package. This expectation is validated by the Elemental accumulated total strain range for the third stabilized thermal cycle contour plots shown in Figure 10-5.

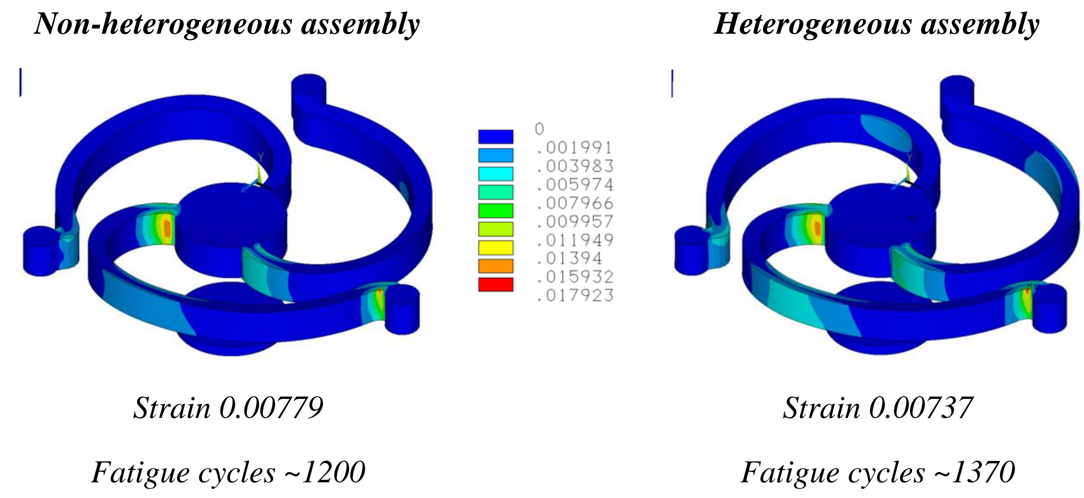


Figure 10-5: Elemental accumulated total strain range for the third stabilized thermal cycle

Plugging in the accumulated strain values from both models into a Coffin-Manson based equation for the prediction of fatigue life, the heterogeneous package has a fatigue life of about 1370 cycles compared to the 1200 cycles predicted for the base model. It can thus be concluded from these results that a heterogeneous configuration of the Delta interconnects not only improves the electrical performance of the assembly but also enhances its thermo-mechanical fatigue life.

Some of the drawbacks with implementing heterogeneity in the package include: the additional design work needed to characterize the variants, to determine what dimensions to make these variants, and the spatial locations to situate them. The die stress and die warpage are somewhat higher than those encountered in the base package, never-the-less, the stress values are relatively low compared to the stresses generated in the die during other CMOS processing steps.

Figure 10-6 is a contour plot comparing the accumulated strains in the finely meshed interconnects in the heterogeneous package. These interconnects represent the farthest interconnects from the neutral point of the die for each of their types. From the plots, the high compliance interconnect has the highest accumulated strains, followed by the intermediate compliance interconnect, and then the low compliance interconnect. Qualitatively, it can be inferred that the interconnect with the greatest likelihood to fail first is the outermost (or high compliance) interconnect, as designed and intended.

Figure 10-6: Accumulated plastic strain range comparison between Delta interconnect variants

10.1.3. Physical Characterization of Heterogeneous Interconnects

To enable physical characterization of the heterogeneous interconnects, die samples were fabricated with each variant of the Delta interconnect laid out as shown in the mask image in Figure 10-7. The low compliance interconnects occupied the inner ring on the die, followed by the medium compliance interconnects which occupied the region between the inner ring and the second ring. The high compliance interconnects occupied the outer region.

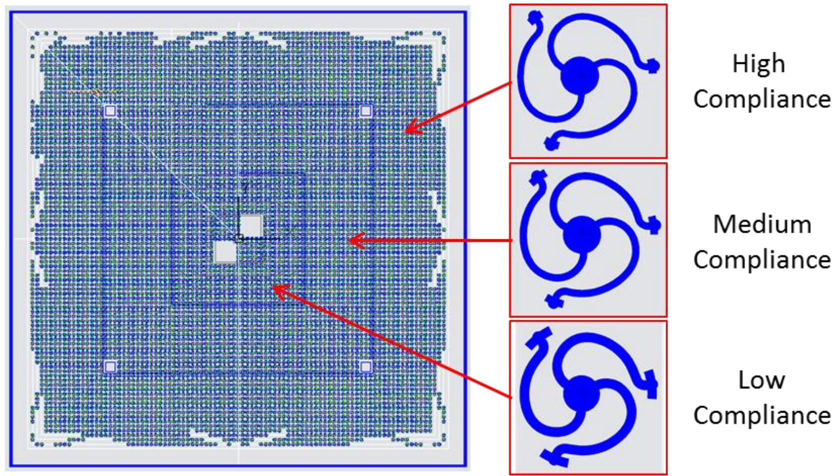


Figure 10-7: Interconnect layout on heterogeneous die

10.1.3.1. Resistance Measurement

Electrical resistance measurements of the three (3) design variants were carried out on an unassembled die. The nature of the test vehicle designed for the characterization of assembled samples did not include test features for characterizing structures within the outer three rows of interconnects. This includes the medium compliance interconnects and the low compliance interconnect.

Using a Signatone® probe station, four-point electrical resistance measurements of the three variants were carried out as described under Chapter 9 – Testing. In these tests, 5 mA of current was used to excite the interconnect, while a voltmeter was used to measure the potential drop across the interconnect. Using Ohm's law, the resistance of the interconnects calculated as a ratio of measured voltage to the applied current are displayed in Table 10-2.

Table 10-2: Measurement interconnect resistances by type

	Primary Structures High Compliance	**Intermediate Structures** Medium Compliance	**Central Structures** Low Compliance
Measured width [µm]	7.2	8.1	11.4
Measured [mΩ]	15.1	13.6	8.9
Simulated [mΩ]	14.7	12.5	8.6

From Table 10-2, it can be observed that the resistance of the centrally placed interconnects are lower by over 40% in comparison with the primary structures. This improvement in resistance and the sturdier build of the central structures enable them handle much higher current densities and dissipate less energy in the process. The intermediate structures illustrated in the table only result in a 10% reduction in resistance. While marginal, this improvement can lead to a reduction of up to 10% in signal delay compared with the base model.

Considering that the measured widths of the fabricated interconnects are much wider than designed by up 20%, simulations using the measured dimensions were created to better match the experimental results. Since these interconnects were batch fabricated, they were assumed to have the same height. A common thickness value of 10 µm was therefore used for the electrical simulations. Comparing the measured data with the simulated values, there is good correlation between the simulated and measured resistance values. Much like the compliance of the interconnects, the resistance values also decline with increasing interconnect widths.

10.1.3.2. Compliance Measurements

Interconnect Variants	Load-displacement curves	Compliance [mm/N]
High Comp		Experiment: 4.96 Simulated range: (30 GPa – 9.346) (200 GPa – 1.402)
Med Comp		Experiment: 3.50 Simulated range: (30 GPa – 7.653) (200 GPa – 1.148)
Low Comp		Experiment: 1.35 Simulated range: (30 GPa – 4.014) (200 GPa – 0.602)

Figure 10-8: Load vs. displacement plot to determine out-of-plane compliance

Using the setup discussed in Section 9.3.1.1. , the mechanical compliance of the interconnects were measured using nano-indentation. The inverse slope of the load-displacement graphs embedded in Figure 10-8 was used to determine the compliances of each interconnect variant. As seen in Figure 10-8, the measured compliance increases from 1.35 mm/N to 4.96 mm/N, as one traverses from the center of the die to the edge of the die. The measured compliance values fall within the range obtained through simulations with electroplated copper modulus varying from 30 GPa and above.

10.2. SCALABILITY OF DELTA INTERCONNECTS

Scalability of the interconnects is an important aspect of their development as it demonstrates the adaptability of the design to different package configurations. This work has primarily focused on 200 µm pitch fabrications. However, some work was also done of 100 µm pitch fabrication as well as 400 µm pitch fabrication.

10.2.1. 100 µm Pitch

To demonstrate scalability of the interconnect design, scaled versions at 100 µm pitch were fabricated using negative photoresists. The 100 µm fabrication was a first iteration of mask design and fabrication procedure. Based on this work, the lessons learned were directly applied in the development of the 200 µm and later 400 µm pitch interconnects for second level applications. One such contribution concerned the design of the original die pad. The initial die pad design conformed with the traditional solid disk available on most soldered packages. With such a design photoresist disks were patterned over the copper pads as shown in Figure 10-9, which were then reflowed to form domes over the copper pads as shown in Figure 10-10. The reflow of the disks was necessary to avoid sharp corners within the arcuate of the interconnect as would be obtained if the interconnects were fabricated over the patterned disks. However, the challenge faced with the reflow process was a difficulty in confining the domes to within designed dimensions. This led to the design of an annular dome in the second iteration of the design process and shown in the 400 µm pitch fabrications.

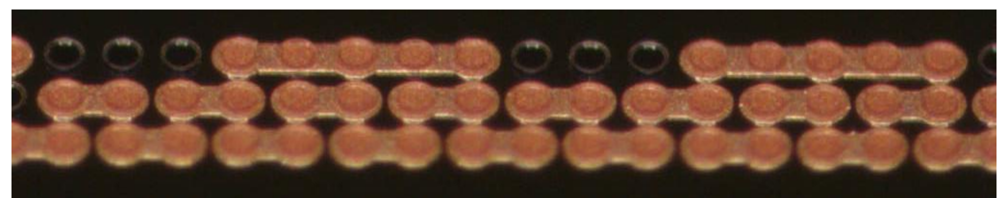


Figure 10-9: Patterned photoresists over copper pads

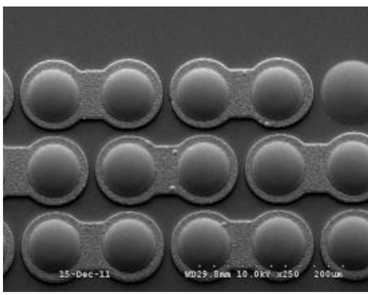
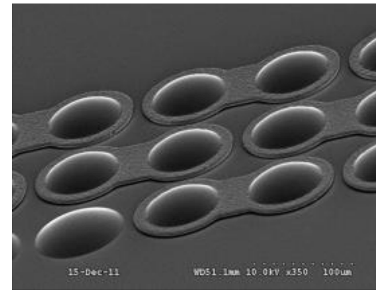



Figure 10-10: Reflowed and metallized domes over copper pads

Figure 10-11 shows an image of fully released successful fabrication of a family of multi-path interconnects. These samples demonstrate the downward scalability of the designed interconnects. For pitch sizes lower than 100 µm, this can be achieved by using a positive tone photoresist. Positive photoresists are known to have much better feature resolutions than negative photoresists [72]. For example, the feature limit of SPR220 as demonstrated by the manufacturer is about 1 µm. Based on this dimension and scaling linearly the 3 µm width 100 µm pitch interconnects, fabrications with pitches as fine as 30 µm is possible.

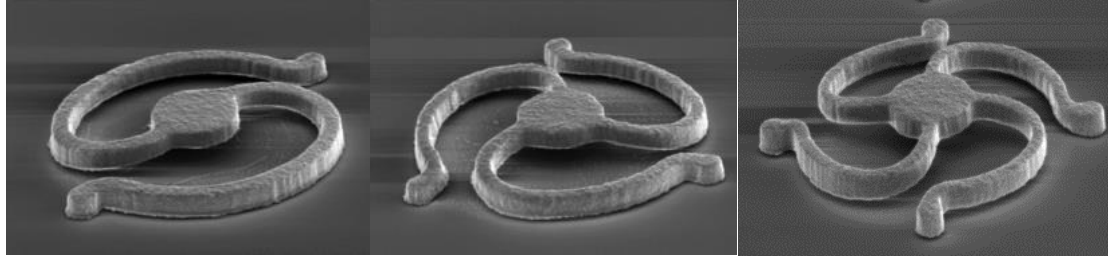


Figure 10-11: 100 µm fabrications showing three multi-path designs

10.2.2. 400 µm Pitch

For second-level interconnects, the Delta interconnects were fabricated on 7 mm dies at 400 µm pitch and also on 18 mm dies at the same pitch. The 7 mm die samples were used for process development ahead of fabrication involving the larger dies. For a scaled up version of the 200 µm pitch Delta connect, the photoresist that we characterized

for the 200 μm fabrication was not capable of meeting the desired thicknesses at the 400 μm pitch successfully. To address this concern, a thicker positive tone photoresist was acquired for the 400 μm pitch fabrication.

The thicker photoresist used for most of the 400 μm pitch fabrications was AZ40XT manufactured by AZ Electronic materials. This photoresist is formulated for thick coats and can easily achieve 60 μm thick films in a single coat. To achieve such thick coats in a single step, AZ40XT was designed to be very viscous. Ordinarily, this did not pose any problems on plain wafers or wafers with a planar surface. However, on non-planar surfaces, such as is created after the plating of the interconnects, trapped air within the features housing the interconnects could not be avoided. The remedy to this problem was the use of a less viscous photoresist to define the solder openings over the copper pads.

With the resolution of the air lock issues arising from the use of AZ40XT over a non-planar surface, samples were successfully fabricated and released. Figure 10-12 shows fabrications without plated solder. Such assemblies require boards with pre-deposited solder for assembly. Figure 10-13, on the other hand, shows fabrications with plated solder on the interconnects. Traditionally, these soldered samples are reflowed to form the plated solder into sphere prior to assembly. The reflow process helps increase the stand-off height of the die from the substrate.

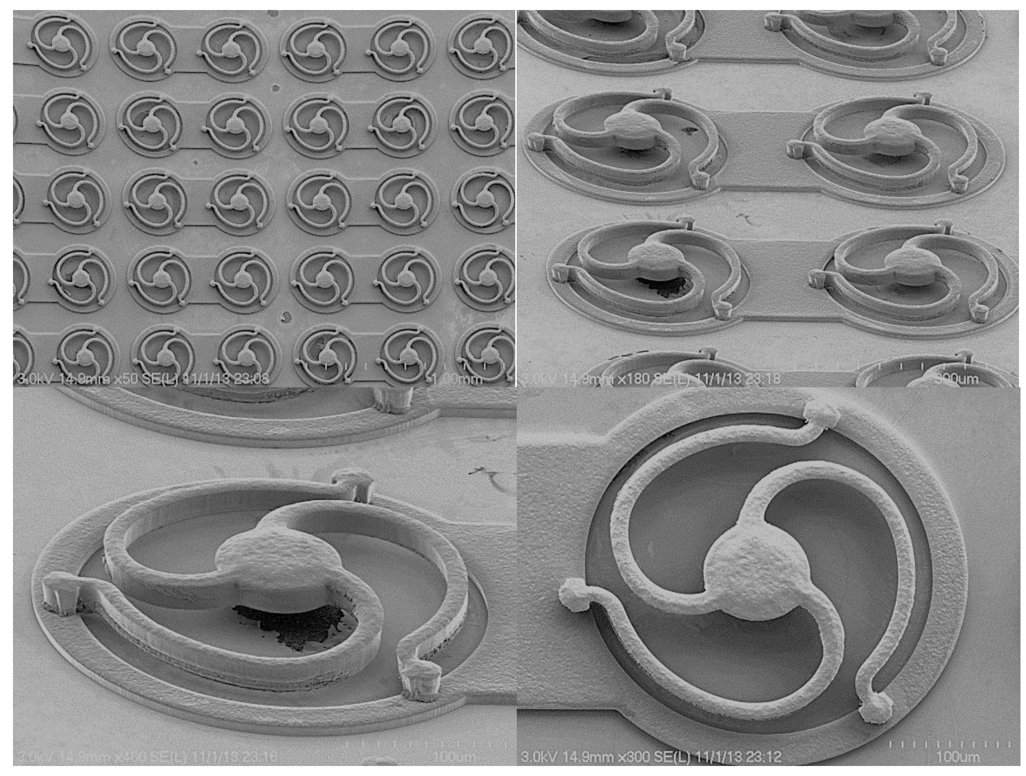


Figure 10-12: Released 400 μm pitch fabrications without plated solder

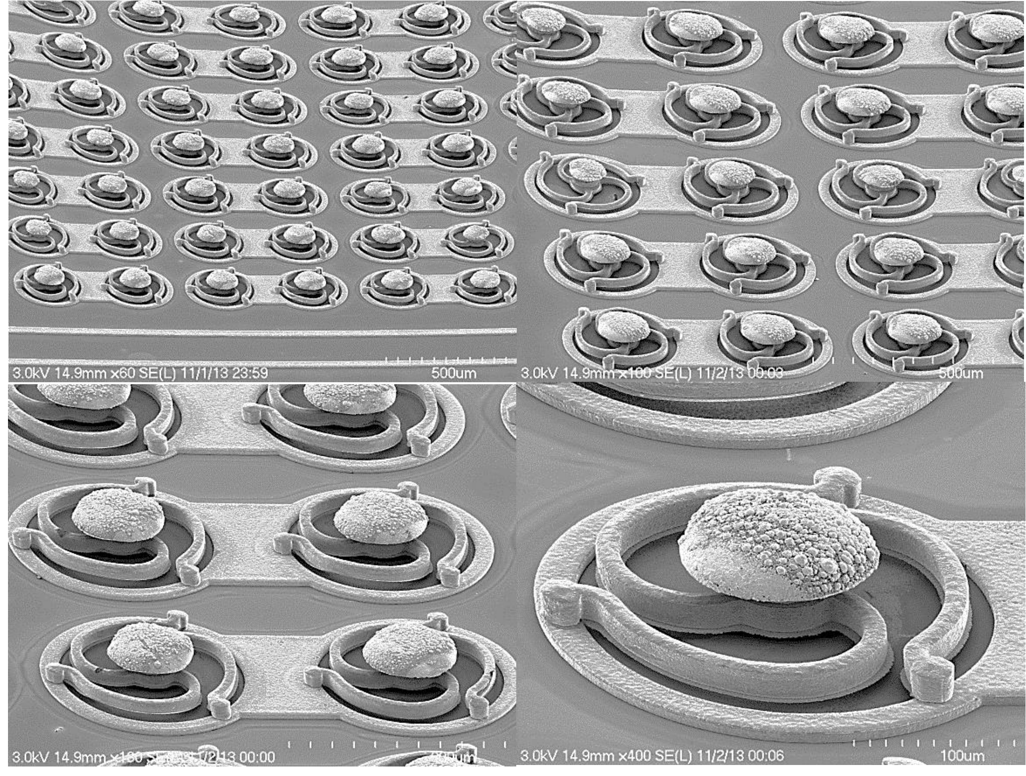


Figure 10-13: Released interconnects with plated solder caps

10.3. CONCLUSION

Through finite element simulations heterogeneity of the Delta interconnects has been explored. Studies show that in a heterogeneous package, slightly larger die stresses and die warpage are encountered as a result of the stiffer interconnect housed within the inner region of such an assembly. The inclusion of the stiffer interconnects improves the overall electrical performance of the assembly as lower resistance pathways are created by the less compliant interconnects. With respect to the reliability of the heterogeneous sample, a slight impact as a result of the larger assembly warpage is observed. The reduction in fatigue life is less than 10% and should not be noticeable in an actual structure.

Through fabrication, the scalability of the interconnect for use in finer pitch applications was demonstrated. These interconnects were also scaled up for use as second level interconnects. This shows the versatility of the design and the capability to adapt it to across different technology platforms. In particular, for applications such as 3D stacked dies and 2.5 D packages where a planar surface is desired for the mounting of die stacks, the low warpage of the Delta interconnects makes them well suited for these applications.

CHAPTER 11

SUMMARY AND CONTRIBUTIONS

11.1. SUMMARY

Several compliant interconnect designs have been proposed to address the copper/low-κ thermo-mechanical reliability issues. A review of existing interconnect solutions revealed several challenges impeding the wide-scale adoption of these solutions. The challenges relate to the difficulty in fabrication or elaborate fabrication procedures, low yield and repeatability of results, challenges with assembly and little to no available data on their thermo-mechanical reliability. The Delta interconnect was developed to address several of these limitations by creating a realizable solution that is cost effective, easy to assemble and thermo-mechanically reliable.

Using finite element simulations, models of the Delta interconnects were created and through a parametric study of the impact of changes in its structural dimensions on its mechanical and electrical responses, a suitable dimension was selected for fabrication and further research.

The design selection process was succeeded by fabrication. Only through fabrication could it be demonstrated that the interconnect design was realizable. For a repeatable fabrication process with good yield, an acceptable photoresist capable of achieving the dimensional features of the selected interconnect design was selected. Through characterization of the photoresist, recipes were developed for photolithographic patterning of the interconnects.

The fabricated interconnects were then subjected to several characterization tests which include electrical resistance measurements, compliance responses, assembly, assembly warpage tests and thermal cycling. In all, the Delta interconnect design has a good balance between its electrical and its mechanical attributes. The primary goals in the development of the Delta interconnect was to develop an interconnect design that is

manufacturable, easy to assemble, and most importantly, that is thermo-mechanically reliable. Through the discussions based on its development, fabrication, assembly and testing, the Delta interconnect, as a proof of concept, has been able to achieve its set goals.

11.2. FINDINGS AND CONTRIBUTIONS

- This work has developed a novel multi-path compliant interconnect that addresses several of the shortcomings associated with other compliant interconnects. The multi-path interconnect has built-in redundancy, and thus, will function, even if one of the paths fails.
- The developed interconnect has an out-of-plane compliance of 5 mm/N and in-plane compliance of at least 1 mm/N, which several orders of magnitude greater than what solder bumps can offer.
- Unlike several other compliant interconnects, the developed interconnects have uniform in-plane compliance, and thus, they can be placed in any orientation on the die.
- Through balanced mechanical and electrical design, this work has shown that the compliant interconnects have a DC resistance of 15 mΩ, and such a resistance is very low for a compliant interconnect, given that it has a high compliance. Such low resistance and high compliance, through experiments and simulations, are rarely demonstrated.
- The developed interconnects create stresses in the die in the range of 1-4 MPa, far lower than the stresses created by underfilled solder bumps. Thus, the proposed interconnects will not crack or delaminate on-chip low-κ dielectrics in next-generation microelectronic devices.
- The developed interconnects use aligned die and substrate pads, and thus, can be a drop-in solution for flip-chip applications.

- This work has developed a comprehensive reflow assembly process for assembling compliant interconnects on organic substrates, and such assembly process for compliant interconnects is seldom found in open literature.
- This work has demonstrated through experiments and simulations that the developed interconnects are thermo-mechanically reliable and can last 1000 cycles at 200 μm pitch for a 20 mm die. It is expected that for smaller dies, the thermal cycling fatigue life will be even greater.
- This work has demonstrated that the developed interconnects are scalable and thus can be used for pitches ranging from 100 μm to 400 μm.
- The proposed interconnects are amenable to achieving varying compliance from the center of the die to the edge of the die, using the same masking process steps.
- The developed interconnects use common cleanroom processes and wafer-level fabrication, and thus expected to be cost-effective.
- The proposed interconnects do not require an underfill material, and thus, the assemblies can be re-workable.

11.3. FUTURE WORK

- Although this work has demonstrated proof-of-concept with limited number of samples, more fabrication and assembly need to be done before it can be widely used.
- This work has not examined the vibration and drop-impact characteristics of the developed interconnects. Such a study will be a separate endeavor.
- This work has demonstrated the use of compliant interconnects as the first-level interconnects, and the interconnects can be used as second-level interconnects, as well as for 3D systems.
- More extensive electrical characterization of the interconnects is needed. Also, electromigration studies will be important to pursue.

REFERENCES

[1] A. Grill, "Low and ultralow dielectric constant films prepared by plasma-enhanced chemical vapor deposition," *Dielectric Films for Advanced Microelectronics,* p. 1, 2007.

[2] B. Chandran, R. Mahajan, M. Bohr, and Q. Vu, "The Mechanical Side of Ultra-Low K: Can it Take the Strain?," *Future Fab International,* pp. 121-124, 2004.

[3] W. Volksen, R. D. Miller, and G. Dubois, "Low dielectric constant materials," *Chemical reviews,* vol. 110, pp. 56-110, 2009.

[4] G. Dubois and W. Volksen, "Low-k materials: Recent advances," in *Advanced Interconnects for ULSI Technology*, ed: John Wiley & Sons, Ltd., 2012.

[5] International Technology Roadmap for Semiconductors, "Assembly and Packaging," ed, 2012.

[6] R. J. O. M. Hoofman, V. H. Nguyen, V. Arnal, M. Broekaart, L. G. Gosset, W. F. A. Besling*, et al.*, "Integration of Low-k Dielectric Films in Damascene Processes," in *Dielectric Films for Advanced Microelectronics*, ed: John Wiley & Sons, Ltd, 2007, pp. 199-250.

[7] L. L. Mercado, S. M. Kuo, C. Goldberg, and D. Frear, "Impact of flip-chip packaging on copper/low-k structures," *Advanced Packaging, IEEE Transactions on,* vol. 26, pp. 433-440, 2003.

[8] Q. Zhu, L. Ma, and S. K. Sitaraman, "Development of G-Helix structure as off-chip interconnect," *Journal of Electronic Packaging,* vol. 126, p. 237, 2004.

[9] R. Dudek, H. Walter, R. Doering, B. Michel, T. Meyer, J. Zapf*, et al.*, "Thermo-mechanical design for reliability of WLPs with compliant interconnects," in *Proceedings of 7th Electronic Packaging Technology Conference, 2005. EPTC 2005.* , 2005, pp. 328-334.

[10] L. Ma, Q. Zhu, T. Hantschel, D. K. Fork, and S. K. Sitaraman, "J-Springs-Innovative compliant interconnects for next-generation packaging," in *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, 2002, pp. 1359-1365.

[11] H. S. Yang and M. S. Bakir, "3D integration of CMOS and MEMS using mechanically flexible interconnects (MFI) and through silicon vias (TSV)," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 822-828.

[12] R. J. Wojnarowski and R. A. Fillion, "General Electric Floating Pad Technology For BGA and Other Mismatched CTE Interfaces," in *SMTA International Conference Proceedings*, 1999.

[13] E. Liao, S. S. Ang, A. A. O. Tay, H. Feng, R. Nagarajan, and V. Kripesh, "Fabrication and parametric study of wafer-level multiple-copper-column interconnect," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 1251-1255.

[14] K. Kacker, T. Sokol, and S. K. Sitaraman, "FlexConnects: A Cost-Effective Implementation of Compliant Chip-to-Substrate Interconnects," in *Electronic Components and Technology Conference, 2007. ECTC'07. Proceedings. 57th*, 2007, pp. 1678-1684.

[15] K. Kacker, T. Sokol, W. Yun, M. Swaminathan, and S. K. Sitaraman, "A Heterogeneous Array of Off-chip Interconnects for Optimum Mechanical and Electrical Performance," *Journal of electronic packaging,* vol. 129, pp. 460-468, 2007.

[16] J. Xu, K. M. Razeeb, S. K. Sitaraman, and A. Mathewson, "The fabrication of ultra long metal nanowire bumps and their application as interconnects," in *Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on*, 2012, pp. 1-6.

[17] R. Tummala, *Fundamentals of Microsystems Packaging*. New York: McGraw-Hill Professional, 2001.

[18] MacDermid, "Wire-bonds, Surface Finishes for Wire-bonding Operations," *<http://electronics.macdermid.com/images/cms_images/ff%20wire%20bond.jpg>*, vol. MacDermid Electronics Solutions, p. Wirebonds, 2013 2013.

[19] C. Joly, "Texte de la présentation de Christian JOLY le 14 Octobre 2004. ," *http://www.feb-patrimoine.com/projet/gcos7/colloque/colloque_cjoly.htm>*, vol. 2013, p. Image Tape Automated Bonding, 2004 2004.

[20] K. Gilleo, *Area Array Packaging Handbook: Manufacturing and Assembly*: McGraw-Hill Professional Publishing, 2001.

[21] C. Jin, S. Lin, and J. Wetzel, "Evaluation of ultra-low-k dielectric materials for advanced interconnects," *Journal of electronic materials,* vol. 30, pp. 284-289, 2001.

[22] C. Feger, N. LaBianca, M. Gaynes, S. Steen, Z. Liu, R. Peddi*, et al.*, "The over-bump applied resin wafer-level underfill process: process, material and reliability," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 1502-1505.

[23] L. Garner, S. Sane, D. Suh, T. Byrne, A. Dani, T. Martin*, et al.*, "Finding Solutions to the Challenges in Package Interconnect Reliability," *Intel Technology Journal,* vol. 9, 2005.

[24] D. L. Smith and A. S. Alimonda, "A new flip-chip technology for high-density packaging," in *Electronic Components and Technology Conference, 1996. Proceedings., 46th*, 1996, pp. 1069-1073.

[25] A. Ibanez and E. Fatas, "Mechanical and structural properties of electrodeposited copper and their relation with the electrodeposition parameters," *Surface and Coatings Technology,* vol. 191, pp. 7-16, 2005.

[26] Y. Zhou, C.-S. Yang, J.-A. Chen, G.-F. Ding, W. Ding, L. Wang*, et al.*, "Measurement of Young's modulus and residual stress of copper film electroplated on silicon wafer," *Thin Solid Films,* vol. 460, pp. 175-180, 2004.

[27] T. Wang, F. Tung, L. Foo, and V. Dutta, "Studies on a novel flip-chip interconnect structure. Pillar bump," in *Electronic Components and Technology Conference, 2001. Proceedings., 51st*, 2001, pp. 945-949.

[28] V. S. Rao, A. Tay, V. Kripesh, C. Lim, and S. W. Yoon, "Bed of nails-100 microns pitch wafer level interconnections process," in *Electronics Packaging Technology Conference, 2004. EPTC 2004. Proceedings of 6th*, 2004, pp. 444-449.

[29] W. Koh, B. Lin, and J. Tai, "Copper pillar bump technology progress overview," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 1-5.

[30] M. Topper, V. Glaw, P. Coskina, J. Auersperg, K. Samulewicz, M. Lange*, et al.*, "Wafer level package using double balls," in *Advanced Packaging Materials: Processes, Properties andInterfaces, 2000. Proceedings. International Symposium on*, 2000, pp. 198-200.

[31] T. Osborn, C. Hunter Lightsey, and P. A. Kohl, "Low-< i> k</i> compatible all-copper flip-chip connections," *Microelectronic Engineering,* vol. 86, pp. 379-386, 2009.

[32] A. O. Aggarwal, P. M. Raj, and R. R. Tummala, "Metal–Polymer Composite Interconnections for Ultra Fine-Pitch Wafer Level Packaging," *Advanced Packaging, IEEE Transactions on,* vol. 30, pp. 384-392, 2007.

[33] T. Hamano, T. Kawahara, and J. I. Kasai, "Super CSP< sup> TM</sup>: WLCSP solution for memory and system LSI," in *Advanced Packaging Materials: Processes, Properties and Interfaces, 1999. Proceedings. International Symposium on*, 1999, pp. 221-225.

[34] P. Elenius and D. H. Kim, "Polymer collar for solder bumps," ed: Google Patents, 2003.

[35] N. Okinaga, H. Kuroda, and Y. Nagai, "Excellent reliability of solder ball made of a compliant plastic core," in *Electronic Components and Technology Conference, 2001. Proceedings., 51st*, 2001, pp. 1345-1349.

[36] J. Li, Q. Ye, A. Cassell, H. T. Ng, R. Stevens, J. Han*, et al.*, "Bottom-up approach for carbon nanotube interconnects," *Applied Physics Letters,* vol. 82, pp. 2491-2493, 2003.

[37] J. Li, Q. Ye, A. Cassell, J. Koehne, H. Ng, J. Han*, et al.*, "Carbon nanotube interconnects: A process solution," in *Interconnect Technology Conference, 2003. Proceedings of the IEEE 2003 International*, 2003, pp. 271-272.

[38] S. Lee, B.-J. Lee, and P.-K. Shin, "Carbon nanotube interconnection and its electrical properties for semiconductor applications," *Japanese Journal of Applied Physics,* vol. 48, p. 5006, 2009.

[39] E. Liao, A. A. O. Tay, S. S. T. Ang, H. Feng, R. Nagarajan, and V. Kripesh, "Fatigue and bridging study of high-aspect-ratio multicopper-column flip-chip

interconnects through solder joint shape modeling," *Components and Packaging Technologies, IEEE Transactions on,* vol. 29, pp. 560-569, 2006.

[40] N. J. Ginga and S. K. Sitaraman, "The experimental measurement of effective compressive modulus of carbon nanotube forests and the nature of deformation," *Carbon,* 2012.

[41] N. J. Ginga, W. Chen, and S. K. Sitaraman, "Waviness reduces effective modulus of carbon nanotube forests by several orders of magnitude," *Carbon,* 2013.

[42] N. Srivastava and K. Banerjee, "Performance analysis of carbon nanotube interconnects for VLSI applications," in *Computer-Aided Design, 2005. ICCAD-2005. IEEE/ACM International Conference on*, 2005, pp. 383-390.

[43] S. Strickland, J. Hester, A. Gowan, R. Montgomery, D. Geist, J. Blanche*, et al.*, "Microcoil Spring Interconnects for Ceramic Grid Array Integrated Circuits," 2011.

[44] C. Krüger, D. Bartelink, T. Fritz, T. Leuerer, W. Mokwa, and U. Schnakenberg, "Micro-springs for temporary chip connections," *Sensors and Actuators A: Physical,* vol. 85, pp. 371-376, 2000.

[45] B. Cheng, E. Chow, D. DeBruyker, C. Chua, K. Sahasrabuddhe, I. Shubin*, et al.*, "Microspring Characterization and Flip Chip Assembly Reliability," *42nd International Microelectronics and Packaging Society (IMAPS),* 2009.

[46] L. Ma, S. K. Sitaraman, Q. Zhu, K. Klein, and D. Fork, "Design and Development of Stress-Engineered Compliant Interconnect for Microelectronic Packaging," *Nanopackaging,* pp. 465-490, 2009.

[47] P. Arunasalam, H. D. Ackler, and B. G. Sammakia, "Smart Three Axis Compliant (STAC) Interconnect: An Ultra-High Density MEMS Based Interconnect for Wafer-Level Ultra-Thin Die," in *Electronic Components and Technology Conference, 2005. Proceedings. 55th*, 2005, pp. 1089-1093.

[48] I. Eidner, B. Wunderle, K. Pan, M. Wolf, O. Ehrmann, and H. Reichl, "Design study of the Bump on Flexible Lead by FEA for Wafer Level packaging," in *Thermal, Mechanical and Multi-Physics simulation and Experiments in Microelectronics and Microsystems, 2009. EuroSimE 2009. 10th International Conference on*, 2009, pp. 1-7.

[49] R. Dudek, H. Walter, R. Doering, B. Michel, T. Meyer, J. Zapf, *et al.*, "Thermo-mechanical design of resilient contact systems for wafer level packaging," in *EuroSime 2006. 7th International Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems.*, 2006, pp. 1-7.

[50] M. S. Bakir, H. A. Reed, H. D. Thacker, C. S. Patel, P. A. Kohl, K. P. Martin, *et al.*, "Sea of Leads (SoL) ultrahigh density wafer-level chip input/output interconnections for gigascale integration (GSI)," *Electron Devices, IEEE Transactions on,* vol. 50, pp. 2039-2048, 2003.

[51] D. Li, D. Light, D. Castillo, M. Beroz, M. Nguyen, and T. Wang, "A Wide Area Vertical Expansion (WAVE< sup> TM</sup>) packaging process development," in *Electronic Components and Technology Conference, 2001. Proceedings., 51st*, 2001, pp. 367-371.

[52] J. Novitsky and D. Pedersen, "FormFactor introduces an integrated process for wafer-level packaging, burn-in test, and module level assembly," in *Advanced Packaging Materials: Processes, Properties and Interfaces, 1999. Proceedings. International Symposium on*, 1999, pp. 226-231.

[53] S. Muthukumar, C. D. Hill, S. Ford, W. Worwag, T. Dambrauskas, P. C. Challela, *et al.*, "High-density compliant die-package interconnects," in *Electronic Components and Technology Conference, 2006. Proceedings. 56th*, 2006, p. 6 pp.

[54] H. S. Yang and M. S. Bakir, "Design, Fabrication, and Characterization of Freestanding Mechanically Flexible Interconnects Using Curved Sacrificial Layer," *Components, Packaging and Manufacturing Technology, IEEE Transactions on,* vol. 2, pp. 561-568, 2012.

[55] E. Liao, A. A. Tay, S. S. Ang, H. Feng, R. Nagarajan, V. Kripesh, *et al.*, "Planar microspring—a novel compliant chip-to-package interconnect for wafer-level packaging," *Advanced Packaging, IEEE Transactions on,* vol. 32, pp. 379-389, 2009.

[56] Q. Zhu, L. Ma, and S. K. Sitaraman, "β-Helix: a lithography-based compliant off-chip interconnect," *Components and Packaging Technologies, IEEE Transactions on,* vol. 26, pp. 582-590, 2003.

[57] G. Lo and S. K. Sitaraman, "G-helix: Lithography-based wafer-level compliant chip-to-substrate interconnects," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 320-325.

[58] G. Mehrotra, G. Jha, J. D. Goud, P. M. Raj, M. Venkatesan, M. Iyer*, et al.*, "Low-temperature, fine-pitch interconnections using self-patternable metallic nanoparticles as the bonding layer," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 1410-1416.

[59] R. Okereke, K. Kacker, and S. K. Sitaraman, "Parallel-Path Compliant Structures as Electrical Interconnects," in *Proceedings of the ASME-IMECE*, 2010, pp. pp. 479-485.

[60] K. Kacker, G. Lo, and S. Sitaraman, "Assembly and reliability assessment of lithography-based wafer-level compliant chip-to-substrate interconnects," in *Proceedings of 55th Electronic Components and Technology Conference, ECTC 2005.*, Orlando, 2005, pp. 545-550.

[61] S. Suresh, *Fatigue of materials*: Cambridge university press, 1998.

[62] J. Banantine, J. Comer, and J. Handrock, "Fundamentals of metal fatigue analyses (chapter 2)," *N Jersey: Prentice-Hall,* 1990.

[63] JEDEC Solid State Technology Association, "Temperature Cycling," in *JESD22-A104D-J*, ed: Joint Electron Devices Engineering Council, 2009, p. 5.

[64] A. S. Prabhu, D. B. Barker, and M. G. Pecht, "A thermo-mechanical fatigue analysis of high density interconnect vias," *ASME Advances in Electronic Packaging,* vol. 10-1, pp. 187-216, 1995.

[65] W. Engelmaier, "Results of the IPC copper foil ductility round-robin study," *IPC Publication,* vol. 947, pp. 66-95, 1987.

[66] R. Iannuzzelli, "Predicting plated-through-hole reliability in high temperature manufacturing processes," in *Proceedings of 41st Electronic Components and Technology Conference.*, 1991, pp. 410-421.

[67] C. Kanchanomai, Y. Miyashita, and Y. Mutoh, "Low-cycle fatigue behavior of Sn-Ag, Sn-Ag-Cu, and Sn-Ag-Cu-Bi lead-free solders," *Journal of Electronic Materials,* vol. 31, pp. 456-465, 2002.

[68] E. Becker, W. Ehrfeld, P. Hagmann, A. Maner, and D. Münchmeyer, "Fabrication of microstructures with high aspect ratios and great structural heights by synchrotron radiation lithography, galvanoforming, and plastic moulding (LIGA process)," *Microelectronic engineering,* vol. 4, pp. 35-56, 1986.

[69] J. Yang, B. Kolasa, J. Gibson, and M. Yeadon, "Self-limiting oxidation of copper," *Applied physics letters,* vol. 73, pp. 2841-2843, 1998.

[70] H. E. Materials. (12/05/2013). *MEGAPOSIT™ SPR™ 220 SERIES PHOTORESISTS*.

[71] E. Kobeda and E. Irene, "A measurement of intrinsic SiO< inf> 2</inf> film stress resulting from low temperature thermal oxidation of Si," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 4, pp. 720-722, 1986.

[72] M. Madou, *Fundamentals of microfabrication: the science of miniaturization*: CRC press, 2002.